MCR-70-120

FLIGHT PACKAGED ONBOARD CHECKOUT SYSTEMS DEVELOPMENT UNIT

FINAL REPORT

NAS9-8000

May 18, 1970

Prepared For

NASA Manned Spacecraft Center
Houston, Texas

Martin Marietta Corporation
Denver Division

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W. J. Wise

W. J. Wise, OCS Program Manager

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Foreword

This document is submitted in accordance with Article XVII B of contract NAS9-8000 and constitutes partial compliance with Paragraph 6.0 of Exhibit D to subject contract.

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I. INTRODUCTION

A detailed evaluation of past space flight performance and a thorough analysis of future planned missions, particularly those involving long-duration and/or deep-space, conclusively confirms the need for an on-line, in-flight test capability. Safety and reliability considerations dictate that this capability be in real-time, as significant transmission delays cannot be tolerated. An On-Board Checkout System satisfies these requirements and, in addition, provides the means for an integrated factory through mission test capability with substantial improvements in cost, reliability, flight weight. System down-time is decreased, resulting in a saving of factory-through-launch process time. Requirements for the specific On-Board Checkout System developed under contract NAS9-4899 were derived from detailed analyses of the Apollo Command and Service Module and the Lunar Module. A second contract, NAS9-6630 (Prototype Digital Test Set), provided for the development of a ground version OCS that incorporated approximately 80% of the OCS circuitry capabilities.

This report documents the results of the design, development, fabrication and test of a Flight Packaged On-Board Checkout Set (OCS), a third contract in the OCS program. This contract, NAS9-8000 extends the Digital Test Set into flight packaged electronics while incorporating recommendations from previous contracts along with modifications and additions to address changing requirements.

There were four areas requiring significant development identified at the start of the contract. These were: A comprehensive set of interactive airborne computer programs, an airborne alphanumeric display device, large scale airborne computer, and an on-board maintainable airborne packaging concept. These were resolved by a "Near English" test community language called "TOOL", a four by four inch 252 character plasma display, an IBM 4 Pi-EP Spaceborne computer and a packaging concept allowing the functional module to be easily removed or placed on the spacecraft wall via a cam latching apparatus.

Section II of this report contains a description of the system developed and detailed developmental results.

Section III contains an evaluation of the OCS with respect to the OCS/(Stabilization and Control System) integration task. This task was set up to provide performance data on the OCS when used to checkout an operational Apollo subsystem.

Section IV contains recommendations for areas of change and areas of study which should be considered in any follow-on effort.

II. SYSTEM DESCRIPTION AND DEVELOPMENTAL RESULTS

A. SYSTEM OVERVIEW

The OCS is a computer-controlled checkout system designed for use in manned spacecraft operations. The system is mounted in a console which simulates a section of a typical spacecraft wall and provides cabinets for the supporting equipment necessary to operate the system in the laboratory (see Figure 1).

The developmental OCS hardware units occupy 5.38 cubic feet and weigh 237.5 pounds exclusive of interconnecting wiring. (This would be part of spacecraft wiring in actual usage.) Operating power from the spacecraft +28 VDC bus is 647 watts. A comparison of these figures against design requirements is shown below:

Parameter	Requirement	Actual
Volume-cu ft	5.28	5.38
Weight-lbs	223	237.5
Average Power-watts	875	647

Initial design requirements were based on power conditioning and data control functions being contained within the user function module. A later trade off of packaging/maintainability determined that the power conditioning and data control function should be packaged separately which required additional physical size.

The OCS hardware consists of eight basic units as shown in Figure 2. These units and their primary functions are as follows:

Airborne Digital Computer (ADC) - An IBM 4 Pi-EP airborne general-purpose digital computer, providing the necessary computer control for the system. This machine incorporates overlapped CPU and I/O operation. An interesting feature of this machine is a set of hardwire diagnostic instructions which provide a high degree of self test with minimal CPU requirements.

FIGURE 1 - OCS MOUNTED ON CONSOLE

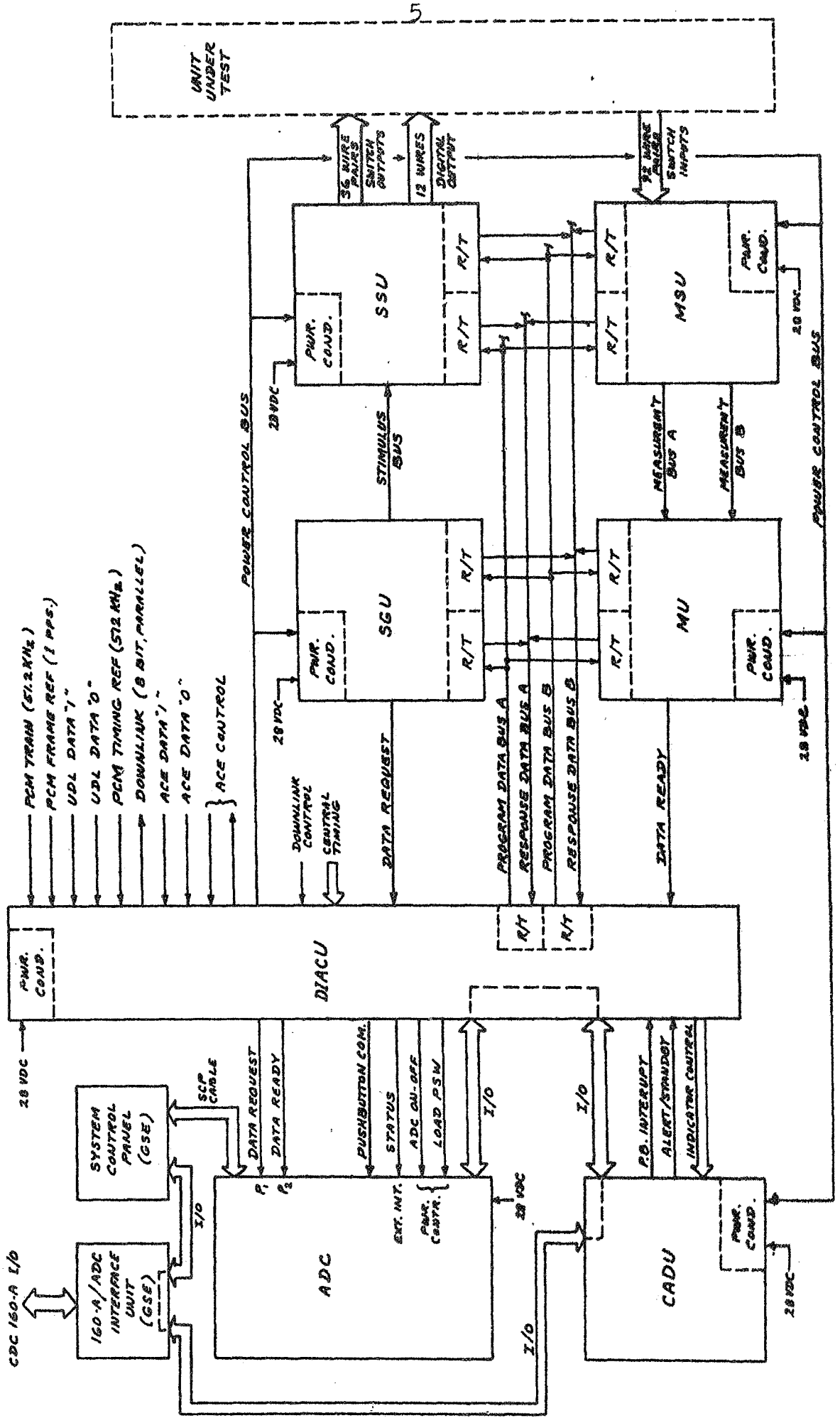


FIGURE 2 - OCS BLOCK DIAGRAM

Control and Display Unit (CADU) - Providing the necessary controls and display devices for the system operator to initiate, monitor, and control the various modes of system operation. The CADU has a direct computer interface and does not utilize the data bus. The CADU contains an alpha numberic keyboard, a graphic/alphanumeric plasma display, a computer controlled microfilm "operators handbook" display, function buttons for system control and a set of system status indicators.

Data Interchange and Control Unit (DIACU) - Providing the interface conversion, timing, and control logic to accomplish data interchange between the ADC and the other OCS units and external data interfaces, providing control of power within the OCS, and controlling CADU indicators to provide display of system status.

Stimulus Generator Unit (SGU) - A programmable function generator, providing analog voltage and current outputs to the analog stimulus bus of the system. The SGU output is floating such that its ground is controlled by the unit under test.

Stimulus Switching Unit (SSU) - A program-controlled signal-switching device used to route analog stimuli from the SGU, internally-generated discrete voltages, and parallel digital signals to selected test points of units under test. The SSU contains special circuitry to detect improper switch operation in order to protect against improper application of stimulus.

Measurement Unit (MU) - A programmable analog signal conditioner and analog-to-digital signal converter, converting analog electrical signals received on the measurement busses to a digital format for interpretation by the ADC. The MU has a high impedance differential input which is electrically isolated such that it assumes the ground potential of the unit under test.

Measurement Switching Unit (MSU) - A program-controlled signal-switching device used to route analog measurements from selected test points of units under test to the analog measurement busses of the system. The MSU contains high speed precision solid state switches for physical size reduction and high reliability.

Power Conditioning/Data Control Module (PC/DCM) - Providing the interface between the remote units and the 28 VDC prime power bus and providing a redundant digital data command and response bus for handling the data interchange between the local and remote portions of the system. This 4 wire twisted pair biphase data bus system eliminates the weight of spacecraft wiring cable bundles.

The system has two basic power states, Standby and Operating. In the Standby state power is applied only to those circuits of the DIACU which monitor for a condition requiring transition to the Operating state and to any CADU indicator lamps that must be on to indicate system status. In the Operating state the computer is on and other functional units of the OCS are energized as required by the functions to be performed. This provides a considerable saving in average system power consumption and an increased system lifetime.

Another feature of the OCS is its ability to incorporate both centralized and built in test concepts. This is possible through the use of the data bus. The block diagram of the OCS as shown is the centralized approach with common stimulus and measurement equipment. However, built in test articles can be attached to the data bus and programmed in the same manner as the centralized equipment.

For purposes of system discussion the OCS units are grouped into Local and Remote categories. The Local group is made up of the ADC, CADU, and DIACU. This group has a fixed structure, whereas the Remote groups may be structured to include any combination of SGU's, SSU's, MU's and MSU's to a maximum of thirty units. The OCS development unit, however, contains only one of each of the four types of remote units.

Both the CADU and the DIACU interface with the Input/Output channel of the computer, the CADU serving as the interface between the computer and the human operator and the DIACU serving as the interface between the computer and the units of the remote group. The DIACU also handles the data interchange between the OCS and external data interfaces such as spacecraft PCM data, spacecraft time, and spacecraft-to-ground and ground-to-spacecraft communication links.

All of the units in the remote group are connected to the DIACU through a redundant set of independent digital transmission systems, either of which is capable of handling the data interchange between the local and remote portions of the system by itself. Each of the transmission systems consists of a Program Data Bus (for conveying computer commands from the DIACU to the remote units) and a response data bus (for conveying measurement data and status information from the remote units to the DIACU for access by the ADC). All units of the remote group receive and transmit bi-phase sinewave data over the transmission systems through receiving, transmitting, and data control provisions contained in their Power Conditioning and Data Control Modules (PC/DCM). The PC/DCM's also provide the interface between the remote units and the 28 VDC prime power bus. The power conditioners contained in these modules are turned on and off selectively by computer commands, via the power control circuitry in the DIACU.

The OCS software consists of four computer program systems; Spaceborne Executive Control System (SECS), Test Oriented Onboard Language (TOOL), Peripheral Interchange Processor (PIP), and Program Preparation System (PPS). The SECS is the executive control system for the OCS software, providing program supervision and scheduling, interrupt control, and utility services. The TOOL system provides the capability for test execution and allows the test engineer to write or review tests from the Control and Display Unit. PIP is a software system used to interface a system-supporting computer with the OCS computer. The PIP system is executed by this supporting computer, a Control Data Corporation (CDC) 160 A or 160 G digital computer. The PPS is executed on an IBM system 360-65 computer and is used in the preparation of the OCS computer programs. The PPS consists mostly of IBM supplied programs.

The OCS has three basic modes of operation: Select, Translate, and Execute. In the Select mode, the operator selects a test sequence and the operation to be performed on it. He may, if the sequence is not contained in the procedure file in computer memory, elect to write that sequence. If the selected sequence is in the file, he may elect to review it by displaying its structure and parameters on the CADU display. These write and review operations are accomplished in the Translate mode. The operator may elect to execute a selected sequence in any one of a number of ways provided by the TOOL test execution capabilities. In the Execute mode the order and nature of computer commands to OCS remote units, computer evaluation of data, and CADU displays depends upon "test element" data in a "test sequence data list" in computer memory. Each test element specifies a specific operation such as a switch closure, a stimulus generation, a measurement conversion, a comparison of measurement data with pre-established limits, a display of results, etc. The OCS has the capability for executing four test sequences concurrently.

To illustrate the general operation of the system we may follow a simple test sequence from inception through execution.

Assume first that the operator desires to perform a simple test on a piece of equipment that involves applying a stimulus to a test point and measuring the equipment's response to that stimulus at another test point. Assume also that there is no suitable test sequence for this specific measurement stored in computer memory. Assume further that the OCS is in the Standby power state.

The operator first presses the ALERT/STANDBY pushbutton on the CADU. This activates "wake-up" circuitry in the DIACU, causing it to signal the ADC to come on and start processing. Now in the "Operating" state, the ADC interrogates the DIACU to determine what caused the state transition. Recognizing that the operator has requested the system, the ADC signals the DIACU to turn on the CADU. The ALERT indicator on the CADU comes on, indicating to the operator that the system is ready to accept his commands.

Next the operator presses the SELECT button on the CADU. This causes the DIACU to signal the ADC that system status has changed. The ADC then interrogates a status register in the DIACU to determine what has happened. Finding that a CADU pushbutton has been pressed, the ADC then interrogates a register in the CADU to find that SELECT has been pressed. It then commands the Microdata Assembly (a microfilm projection device in the CADU) to select and project a film frame containing test instructions to the operator. These instructions are called "Cues". They provide the operator with a list of elective operations and instructions for their initiation.

In accordance with the cue presented on the Microdata Assembly (MA), the operator enters a sequence name via the CADU keyboard. This entry is displayed back to him on the Alphanumeric Display Unit (ADU) contained on the CADU display panel. Also, another cue is presented on the MA. This cue tells the operator that he has selected a sequence that is not contained in the procedure file and informs him of the first operation necessary to write the sequence. The operator then proceeds to write the desired sequence by entering test element names and modifiers on the keyboard. In this process he is cued continuously by the MA and checks his entries with the ADU display. The keyboard entries are translated by the TOOL software into data in the test data list.

At any time in the process of writing the test sequence the operator may elect to review and edit it.

Once complete, the sequence may be executed immediately by pressing either RUN CONTINUOUS or RUN SEGMENT on the CADU keyboard. The primary difference between these two methods of test execution is with the execution of the display element. Only specially designated displays are executed in a continuous run, whereas all displays are executed in a segmented run.

Suppose that the operator has constructed a sequence of the test elements "Begin", "Connect", "Stimulate", "Measure", "Display", and "End". When the operator presses one of the RUN buttons the TOOL software locates the test sequence data list for the selected test in the ADC memory and "begins" the interpretive execution process. First the SSU is commanded to connect the stimulus bus from the SGU to the assigned test point. Then the SGU is set up by a series of commands to supply the selected stimulus to the stimulus bus. The MSU is then directed to connect the assigned measurement test point to the measurement bus. Next the MU is set up to convert the specified type of measurement to digital data. Upon completion of the measurement conversion, the MU signals "Data Ready" to the ADC. The ADC then commands the MU to transmit the data to it via the DIACU, formats the data for display, and commands the CADU to display the test result. Another press of one of the RUN buttons ends this test sequence execution.

The next subsections of this report document detailed developmental results on each OCS unit.

B. AIRBORNE DIGITAL COMPUTER (ADC)

MMC, in conjunction with NASA-MSC made a computer survey to determine the availability of a flight qualified (or in process thereof) digital computer which would meet the current and projected OCS requirements. Availability within the constraints of this contract resulted in the selection of the IBM System/4Pi, Model EP computer. This unit had been previously selected for a manned AIR FORCE program and thus was currently under production. (AIR FORCE program was subsequently cancelled and thus the computer has not been flight qualified, though no problems are foreseen in this area.)

The 4 Pi/EP is a high performance digital computer designed for spaceborne applications requiring real-time processing of large volumes of data. Some of its general characteristics are given below:

a) 72 basic instructions
b) basic cycle time of 417 nanoseconds
c) storage cycle time of 2.5 microseconds
d) addition time of 2.1 microseconds
e) multiply time of 9.2 microseconds
f) division time of 20.0 microseconds
g) instruction word length - 16 or 32 bits
h) data word length - 16 or 32 bits
i) organization - parallel fixed point, 2's complement notation
j) memory size - 16K by 36-bit expandable 131K

The unit is housed in a rectangular case 19.5 inches by 24.5 inches by 9.25 inches. Except in the power supply area, there are two layers of hardware, one accessible from a front cover and the other accessible from a rear cover. The external connector interface is located on the front of the power supply area (See Figure 3). The unit is cooled by circulation of chilled water through a self-contained cold-plate system. As delivered for the OCS usage, the unit weighs approximately 94 pounds.

As noted above, the basic 4 Pi/EP contains a memory capability of 16K by 36-bits. These 36 bits are 4 8-bit data bytes plus an associated parity bit. The memory addressing system is setup for expansion to 131K maximum; however, within the case size identified, a memory size of 24K is maximum. The OCS unit has a 24K memory size.

This computer operates on +28 VDC and requires an average of 14 amperes operating and less than 1 ampere in standby. It has a self-contained voltage sensor for monitoring the 28 VDC input bus. An out-of-limits condition causes the computer to immediately store the operating conditions and shutdown. Return of normal input voltage will allow the operator to resume operations or, in the case of OCS, allow the next wake-up function to operate correctly.

Logic hardware is IBM specified TTL built primarily by Texas Instruments, Inc., and thus is directly compatible with the OCS hardware selection. Memory planes are militarized system/360 designs. The Read Only Store (ROS) memory module contains the machine instruction repertoire which is hardwired in at time of assembly. That is, to change instructions, it is necessary to make a new ROS module. The machine language is System/360 compatible and thus 4 Pi/EP programs can be assembled and verified on System/360 computers.

The I/O is also System/360 compatible. Thus a 4 Pi/EP can be connected to System/360 peripherals in a ground-based installation. The I/O is a single multiplexer channel, is 8-bit byte oriented and has four modes of operation: Multiplex, burst, lockout and direct input/outout. In the multiplex mode, each controller (maximum of eight) on the channel is allowed to transfer one byte of data (either way) if it wants to do so; otherwise it is bypassed and the next one in sequence may do so. Thus priority of external controllers is determined by their location on the channel. If a higher order controller has a request pending it will be serviced as soon as the channel is relinquished by the current user. Thus there is very little delay in servicing any controller on the channel.

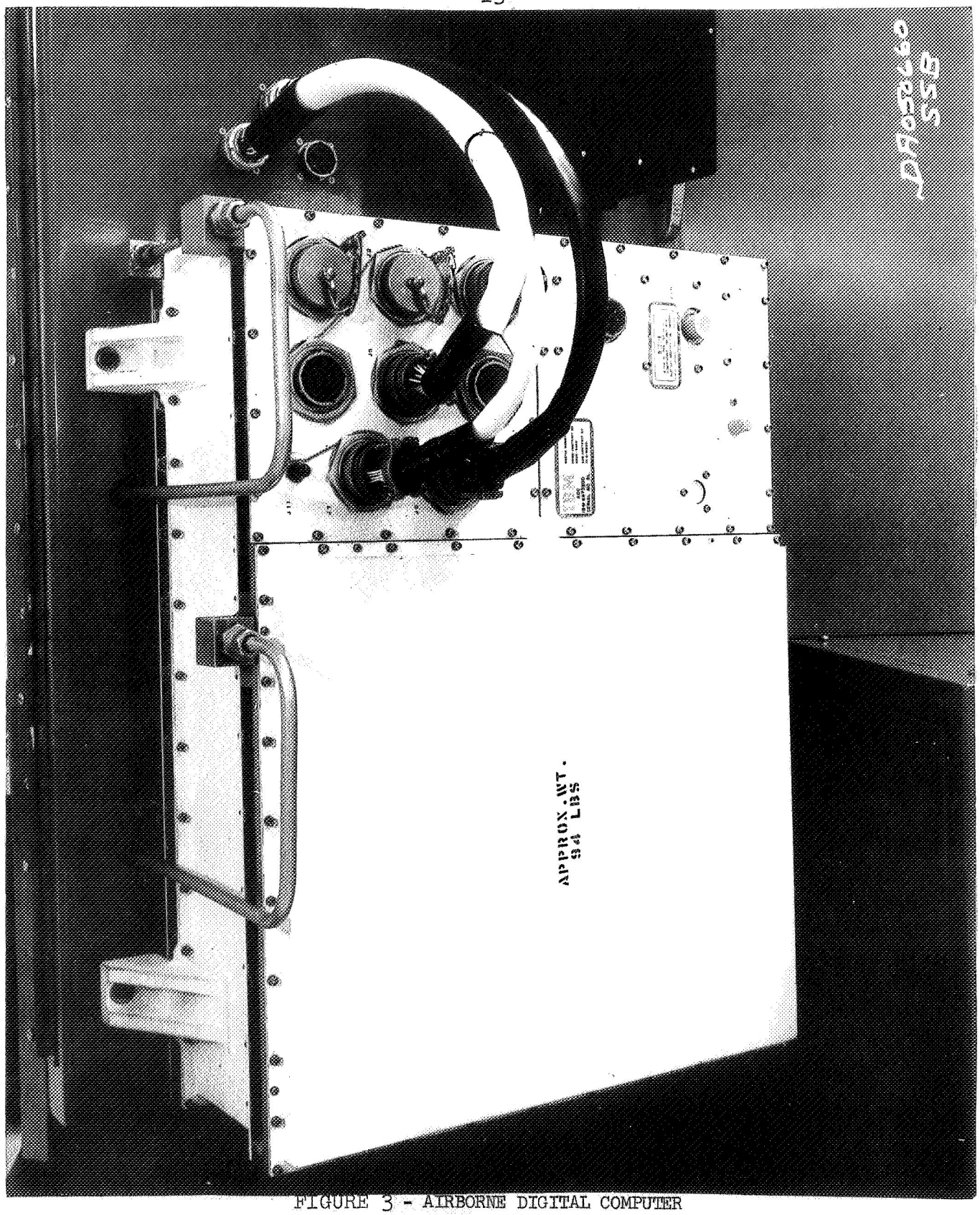


FIGURE 3 - AIRBORNE DIGITAL COMPUTER

In burst mode, however, a controller has the channel tied up for a specific number of byte transfers. Such operation is required for mass storage transfer of programs or data tables and for display/keyboard devices. Lockout mode is the same as burst except the CPU is also tied up. In both multiplex and burst modes the CPU is only tied up during the actual byte transfer time.

The final mode, Direct I/O, is a means of transferring two or four byts of data between a device and the CPU directly under control of a CPU instruction. This also ties up the CPU for the duration of the operation.

Although each individual system incorporating a 4Pi/EP must be analyzed to obtain its specific data transfer rates and associated CPU interference times, typical values are:

Data Rate	CPU Interference	Mode
18KB	25%	Multiplex
36KB	50%	Max. Multiplex
115KB	75%	Max. Burst
400KB	100%	High Speed

As stated above, the 4Pi/EP also has a priority interrupt system. This contains 6 interrupt levels. Each level may be individually masked by a machine program thus allowing or not allowing external interrupts as desired. As will be noted later the OCS only uses three external interrupts: DIACU, SGU and MU.

The 4Pi/EP has been in operation for about 2800 hours and has experienced two failures. Failure one was a flat pack AND/OR gate at about 1000 hours operation. Failure two was a marginal sense amplifier in the read only store.

The 4Pi/EP is compatible (instruction repertoire) with the IBM 360 system. This compatibility allowed all software to be written with the use of the 360 assembly language and assembled on the 360 hardware.

The 4Pi/EP instruction repertoire as stated previously is compatible with the IBM 360. Since the 360 is basically a business data processing system the repertoire has shortcomings for a real-time application. Specifically, the 16 general purpose registers as they are used in the 360 do not allow efficient real time program relocation in core memory. An approach involving a single relocation register such as is utilized in the CDC 6000 series machine should be investigated.

The 4Pi/EP has 6 priority interrupts. This number should be expanded to a minimum of 16. This would save the overhead of software decoding of the interrupt.

Another set of instructions which would better address the real time problem is a set of stack manipulation instructions. This would allow queues, real time stacks, and lists to be manipulated without extensive software.

The 4Pi/EP architecture contains a "WAIT" state which was utilized by the OCS. The WAIT state uses minimal computer power which is about 125 watts less than fully computing. This has proven to be an excellent feature and reduced the average OCS power consumption.

The 4Pi/EP multiplexer Input/Output channel is also 360 compatible. The channel is basically for devices which transfer bursts of data periodically. This single channel poses problems for the OCS when the single channel decom is running concurrently with other OCS activities such as plasma display etc. In order to relieve this problem the EP must be set up to handle multiple I/O channels including a selector channel.

The EP contains in its repertoire a set of DIAGNOSE instructionswhich are used for a high speed low overhead self test. This has proven to be excellent for detecting machine failures in the real time mode.

The EP weighs 94 lbs, uses 1.9 cubic feet and requires an average power of 347 watts.

C. CONTROL AND DISPLAY UNIT (CADU)

The CADU is the man-machine interface of the OCS. As shown by Figure 4, it provides a display panel with two display screens, groupings of discrete-message indicators, and a row of function-control pushbuttons. In addition, the CADU contains a slide-away keyboard which is secured in the stowed position with cam-action latches. By releasing the latches and pulling forward the keyboard slides out and locks into position for use as shown in Figure 5.

The two display screens are the Alphanumeric Display Unit (ADU) and the Microdata Assembly (MA) discussed below. The discrete message indicators are incandescent lamp type, computer controlled and powered from the DIACU Standby/Alert Indicator power supply. This allows discrete messages to be displayed even though the CADU is powered down.

The keyboard contains a group of alphabetic, numeric, and symbolic character pushbuttons similar to those on a standard typewriter keyboard. Included in this grouping are buttons for keyshift, space, and backspace as on a typewriter. A "clear" function is also included. On the right of the keyboard, a group of 15 buttons is provided for OCS function control.

Except for the display devices, the unit is contained in a machined magnesium case with separate bays for power supply, electronics module, and keyboard stowage. The top of the case serves as a cold plate and mounting surface for the modules within the case and for the display devices which mount on top of the case. The Alphanumeric Display Unit is mounted on the left of the case top and the Microdata Assembly mounts on the right.

The pushbutton switches are all recess-mounted so that deliberate action is required to depress more than one switch. Sixty-three of the pushbuttons operate to set individual "interrupt status" flip-flops on key-down (normally open contact) and reset it on key-up (normally closed contact). The interrupt status flip-flops are grouped into sets to form eight 8-bit bytes in a 64-bit keyboard interrupt register (1 bit of the register is not used) as shown in the CADU block diagram, Figure 6. The presence of a true state on any one of these flip flops causes an interrupt signal to be sent to the DIACU. Then, through a process to be described in the DIACU discussion, the ADC recognizes that a pushbutton has been pressed and commands the computer I/O interface. The transmission is accomplished in eight bytes, which the ADC interrogates to determine which pushbutton was pressed.

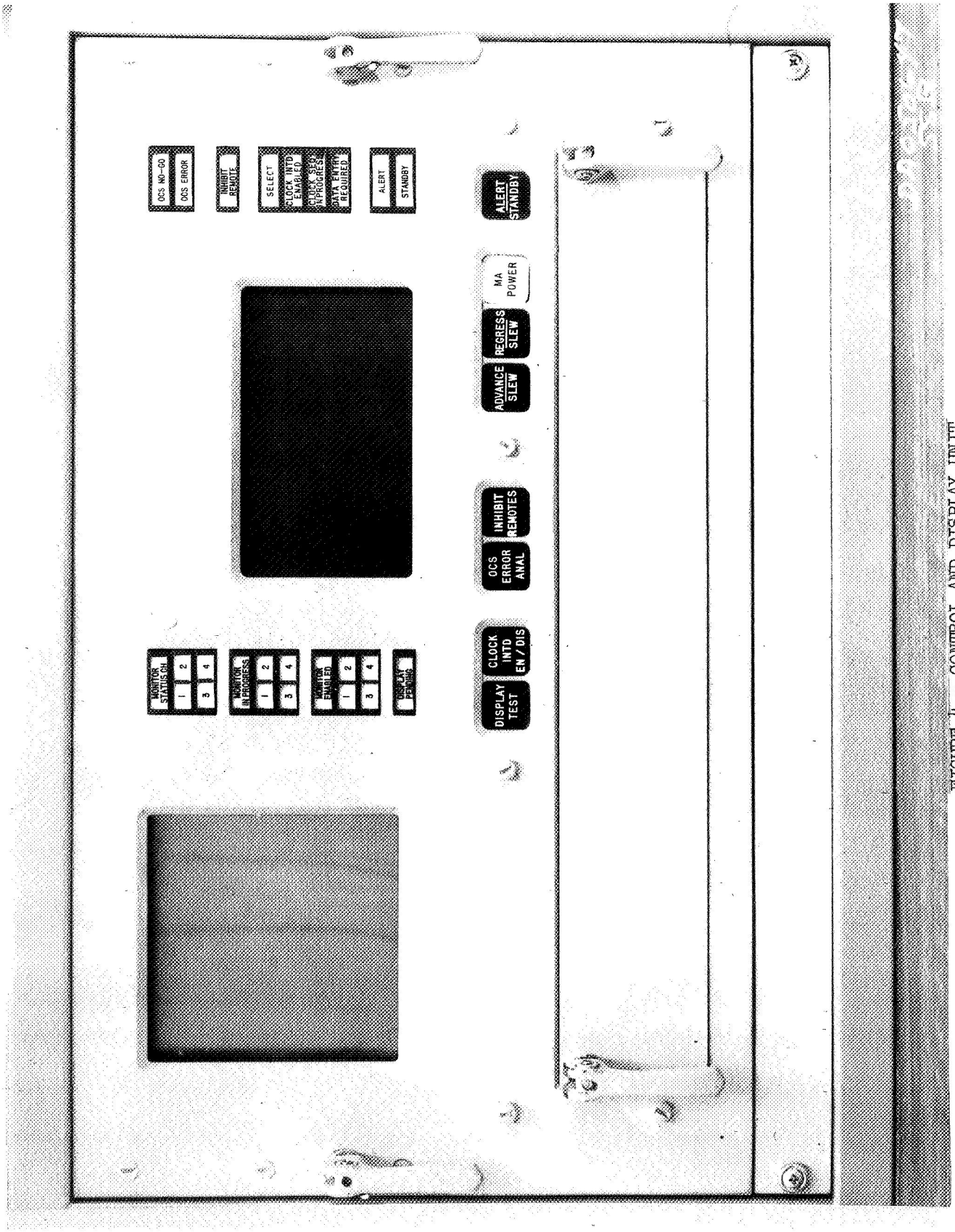


FIGURE 4 - CONTROL AND DISPLAY UNIT

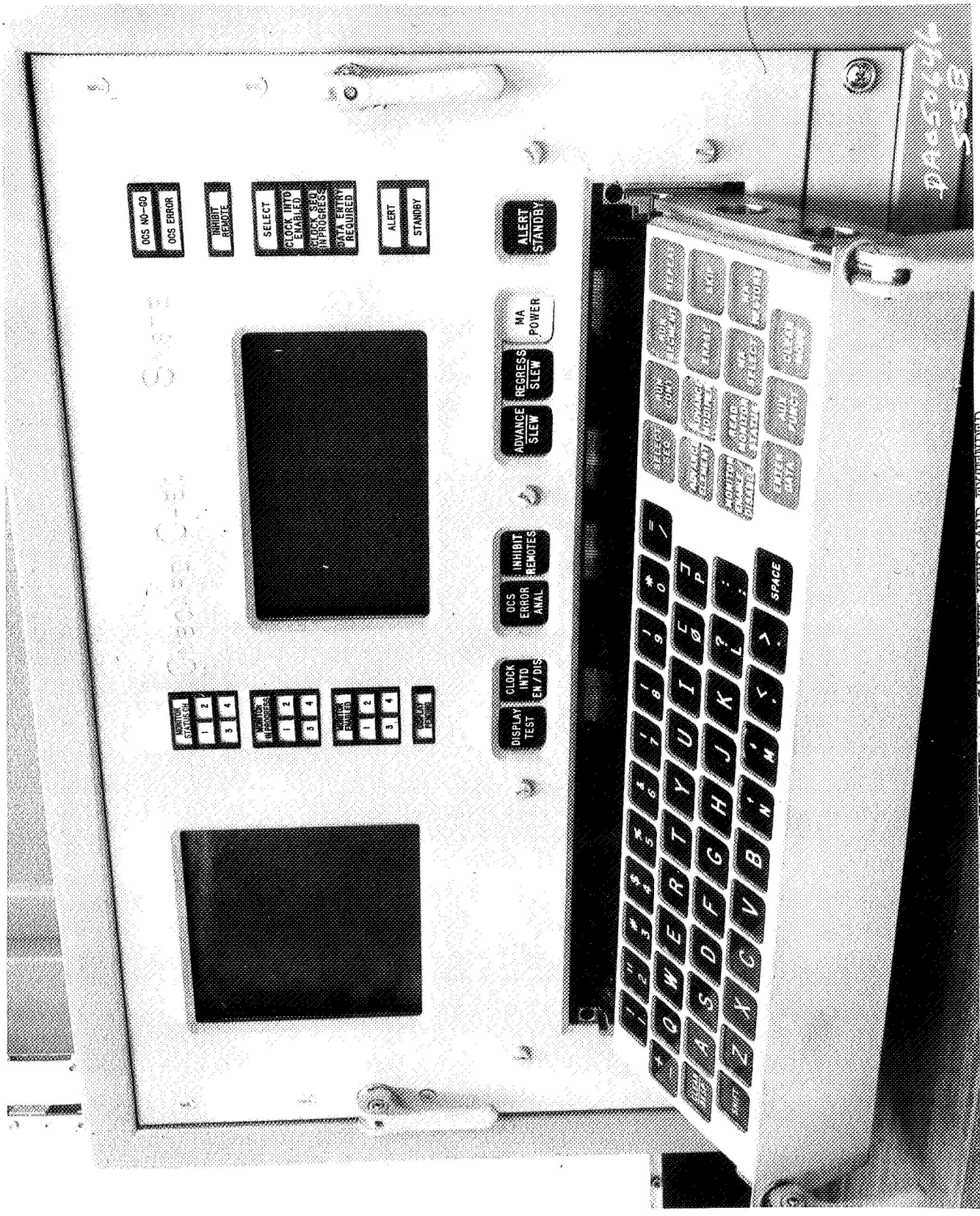


FIGURE 5 - CADU WITH KEYBOARD EXTENDED

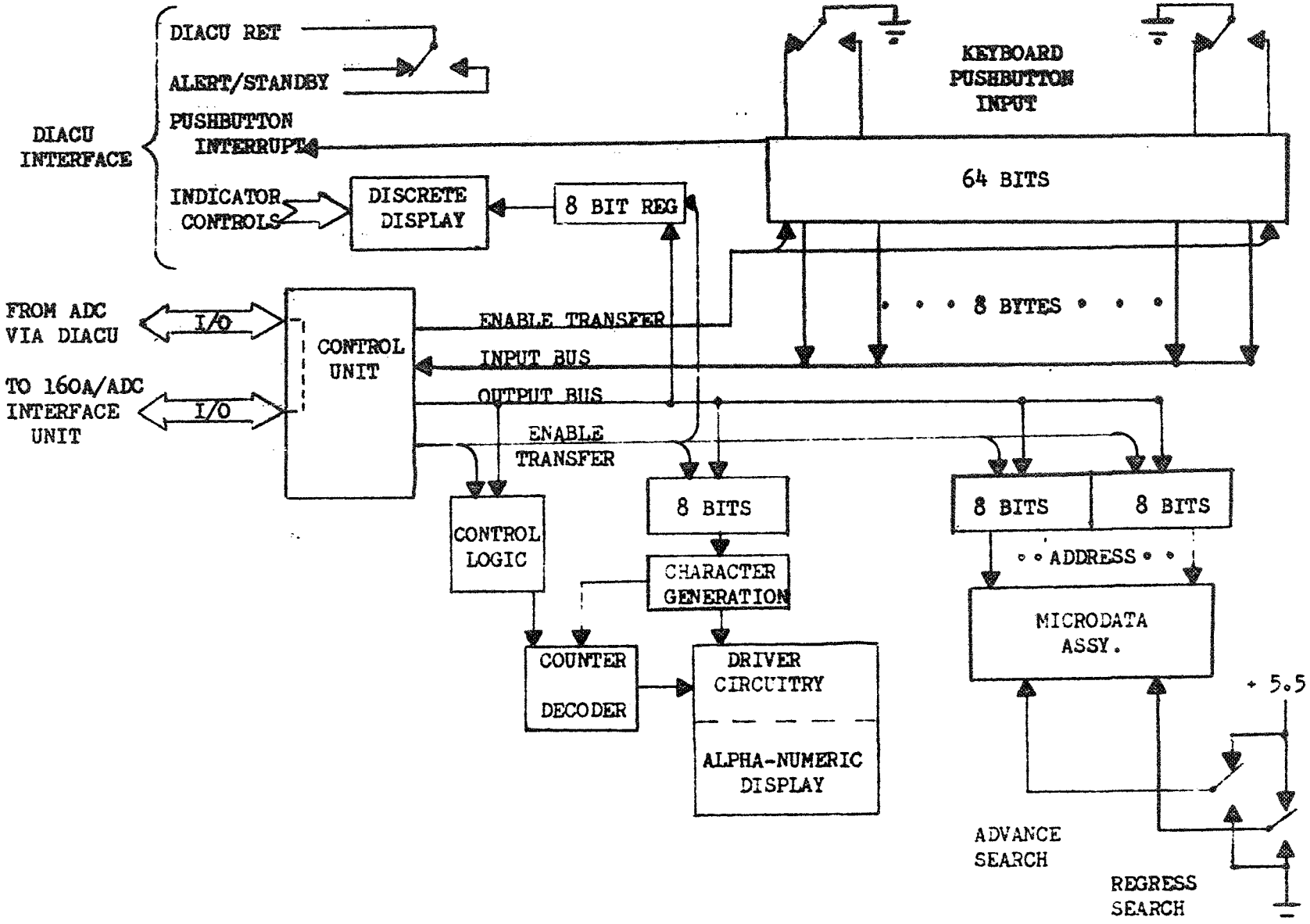


FIGURE 6 - CADU BLOCK DIAGRAM

The pushbutton switch labeled ALERT/STANDBY is used to signal the DIACU when the operator desires CADU power on or off. The normally closed contact of this SPDT switch switches an "Alert/Standby Off" line from the DIACU to the "DIACU Return" line. Its normally open contact, on key-down switches the "Alert/Standby On" line from the DIACU to the DIACU return line. The DIACU response to the above actions will be described in the DIACU section.

Microdata Assembly (MA), is a self-contained three-piece assembly containing an electronics module, a tape casette, and a light module. The light module fits into the tape casette which then fits into the MA case. When programmed from the computer via a 16 bit MA control register in the CADU electronics, the MA selects and projects the designated microfilm frame. To allow operation of the MA in the event of computer or transmission failure, three special CADU pushbutton switches are provided. These are labeled MA POWER, ADVANCE/SLEW and REGRESS/SLEW. The MA power switch provides manual application of power to the MA only. A momentary contact of the ADVANCE/SLEW pushbutton directly commands the microdata unit to advance the microfilm one frame position. Holding the button down will cause the microfilm to slew forward until the button is released. The REGRESS/SLEW pushbutton performs a similar function, but the film moves in the reverse direction.

The Alphanumeric Display Unit (ADU), provides visual readout of computer-directed alphanumeric messages. The ADU consists of a 4 by 4 inch gas-discharge (plasma) display panel and supporting electronics, framed in an airtight aluminum box. The display panel contains 15,360 separate gas cells in a matrix 128 cells wide and 120 cells high. Characters are displayed in dot patterns made of 5 by 7 cell arrays in rows, to form twelve 21-character lines. Three horizontal rows and one vertical column of cells are used to space characters. The power supply for the prototype ADU used in the OCS is not contained in the CADU but is mounted in the right hand supporting equipment cabinet of the OCS console.

The CADU electronics is powered from a 5 volt power conditioning module, having circuitry identical to the power conditioners provided in the remote unit PC/DCM's, but repackaged to fit the CADU housing. It has the same provisions for selective power enabling and disabling that are provided in the remote units. CADU power turn off, however, is via a signal from the DIACU over a separate CADU power disable line.

The following paragraphs document development results on the CADU.

The CADU electronics is packaged in the bottom of the CADU chassis. The five metal core printed circuit boards are interconnected through a mother board arrangement.

After initial installation of the electronics an intermittent was detected. The intermittent was found to be a hair line fracture on a PC board. The mother board did not present as much rigidity as anticipated so it was braced with phenolec spacers. This improved the rigidity problem which will also reduce future ribbon fractures. It is recommended that board size be reduced to prevent unwanted flexure in future electronic chassis.

No failures have been experienced in the CADU electronics since initial installation.

The computer controlled microdata assembly had three developmental problem areas.

In order to establish a "point source" lamp in the MA a Xenon source was selected. This unit is manufactured by Pek Laboratories. Difficulty in starting the lamp has required MMC to study different lamps and starting techniques. The unit as a light source is excellent.

A focus problem with the MA has indicated that further development is necessary in the film gate and lens area. The focus of the unit is adequate but can be improved.

The plasma display device is one of the show pieces of the OCS. The first plasma delivered utilized a character scheme in which the background was bright and the character was dark. This unit was hard to read and soon was plagued with dot dropout.

CDC produced a second unit which utilized a bright character and black background. This unit was far superior to the first. After two months use a selective aging of the plasma dot matrix caused a dot drop in and dot drop out fault. In order to cure this CDC built another plasma with uniformly aged dots and with two pulsed bars at the top and bottom of the screen for a source of free electrons. Also each drive or selection wire to each dot was the same length.

With the exception of an occasional problem with lack of free electrons this scheme worked satisfactorily. CDC is working an approach where a light source is used for additional free electrons.

There are two areas which need further development which are not related to the above. A selective erase capability on a character or line basis is necessary to avoid screen blink. The blink was found to be annoying and limited the display speed while requiring additional computer I/O bandwidth. Also the power supplies required for the plasma were packaged in commercial form rather than airborne in order to meet delivery schedules within acceptable technical risk. It is anticipated that these supplies can be packaged within the basic plasma module.

In summary the plasma display presented a very impressive approach to airborne alphanumeric/graphic displays with attendant low power, weight volume and maintainable packaging approach.

The CADU alphanumeric keyboard was initially required to be operated by an astronaut's gloved finger, hence, requiring a beasel to avoid pressing of more than one key simultaneously. After this requirement was established a turn towards the shirt sleeve environment requires that a typewriter compatible feel be achieved which indicates no beasel on future keyboards.

The sliding keyboard arrangement seems to be a fertile ground for comments. Recent onboard systems specifications indicate no protruding devices.

The CADU weighed 53 lbs, and required 73.6 watts and uses 2371 cubic inches.

D. DATA INTERCHANGE AND CONTROL UNIT (DIACU)

The primary function of the DIACU is to provide signal conversions, timing, and control to accomplish data interchange between the ADC and the OCS remote units and between the ADC and spacecraft timing, PCM data, and communication systems. In addition, it provides control of power within the OCS, controls and powers CADU indicators, routes the CADU pushbutton interrupt signal to the ADC, provides the ADC with a time reference, and performs a "watchdog" function to safe the system in event of ADC failure. The unit is packaged in a magnesium case designed to mount on a spacecraft coldplate. Figure 7 presents a block diagram of the DIACU.

The ADC transmits command data to the OCS remote units through the DIACU. When directed by the proper computer command, the DIACU transfers data from the computer I/O channel into the computer-selected one of two 24-bit program data output registers, in 8-bit bytes. The contents of the loaded register are then transmitted serially to the remote units over the program data bus associated with that register.

Serial binary data received from the remote units over the response data bus of either of the transmission systems, is shifted into the associated one of two DIACU response data input registers as it is received. Upon direction from the ADC, the DIACU transfers the contents of either of the response data input registers to the computer I/O channel in 8-bit bytes plus parity.

The DIACU interfaces with the Spacecraft Acceptance Checkout Equipment (ACE-S/C) Uplink, via the ACE-S/C Guidance and Navigation Buffer Unit, to accept 24-bit serial data words into a 24-bit uplink data register in the DIACU. The last bit count of a data word from the Uplink sets an interrupt status bit in the DIACU interrupt status register and causes a "buffer busy" signal to be sent by the DIACU to the ACE-S/C Receiver Decoder. Upon direction from the ADC, the DIACU transfers the contents of the uplink data register to the computer I/O channel.

The DIACU accepts 8-bit data bytes from the computer I/O channel and transfers them in parallel directly to the spacecraft PCM encoder for transmission on the spacecraft downlink. A control line from the PCM encoder signals the DIACU of the acceptance of a data byte.

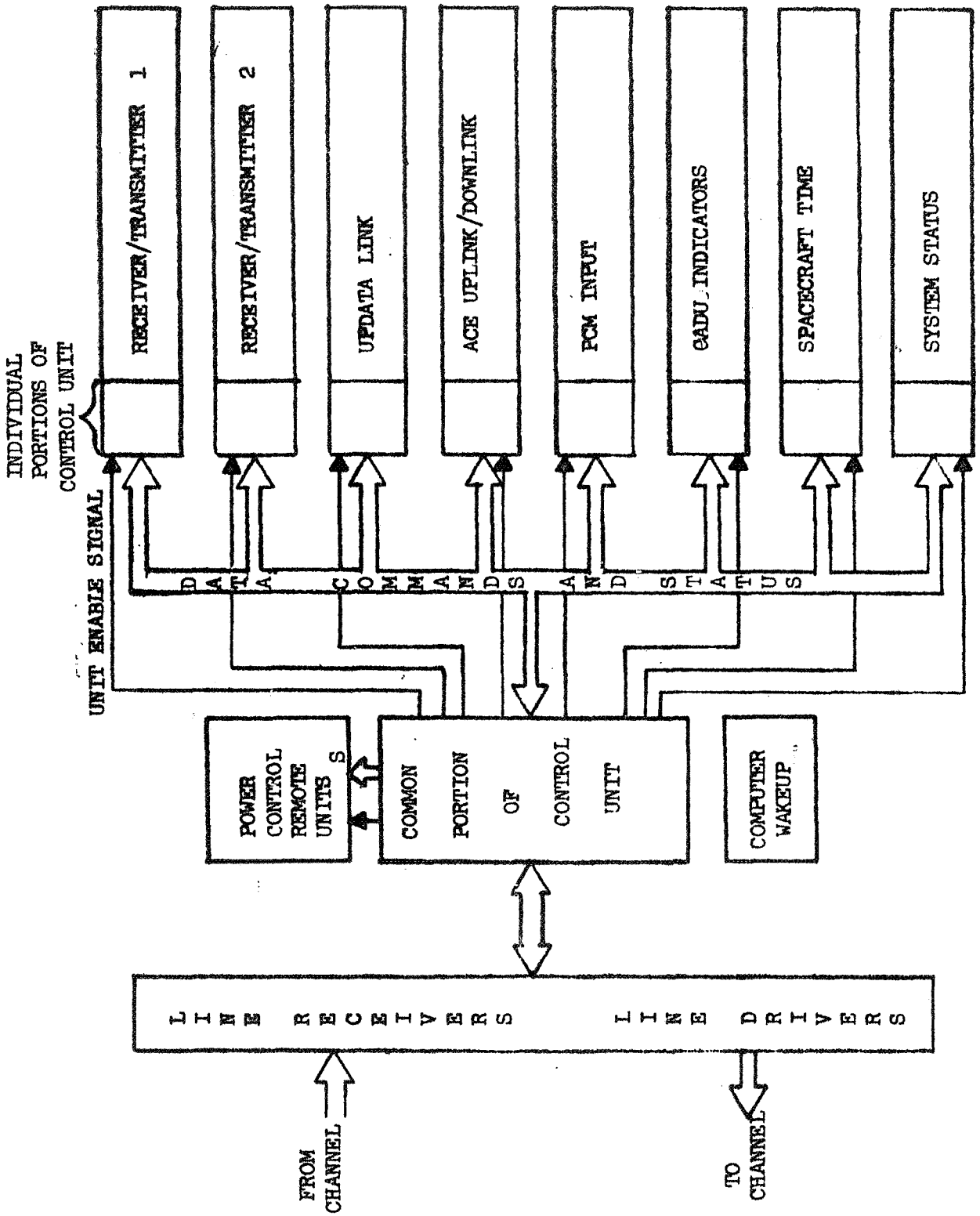


FIGURE 7 - DIACU BLOCK DIAGRAM

An updata channel input to the DIACU comes from the spacecraft command receiver, allowing the DIACU to accept 24-bit serial data from the receiver. This data is accepted at a 1 KHz rate and is held in a 24-bit UpData Link (UDL) input register in the DIACU. When this register is loaded a status bit is set in the DIACU interrupt status register. Upon computer command the contents of the UDL input registers are transferred to the computer I/O channel.

A 16-bit PCM address register is provided in the DIACU. This register can be loaded by the computer to specify the starting prime frame and time slot of PCM data and a data byte sampling rate. Then, upon receipt of the next 1 pps PCM timing reference signal from the spacecraft PCM, the DIACU will count frames and time slots from the PCM 512 KHz timing reference until these counts compare with the address register. The DIACU will transfer successive PCM data bytes, at the selected sampling rate, into the ADC memory until commanded by the computer to cease. Storage for 400 successive PCM data bytes is provided in the ADC memory. Sample rates that can be programmed are 1, 10, 50, 100, 200 and 400 samples per second. Acceptance of all PCM words in the data stream can also be commanded.

Interface with spacecraft time is through a 26 line input to the DIACU. These lines provide the DIACU with time measured in days, hours, minutes, and seconds. The one second period provided by the spacecraft time interface is broken into one millisecond periods by an internal oscillator in the DIACU which drives a counter capable of counting to 999. This counter is reset to zero on the trailing edge of the spacecraft time seconds signal and then counts at a 1 KHz rate until again reset.

Under normal operation the spacecraft time binary coded decimal information is transferred into a storage register in the DIACU once a second. Failure to receive a new time at the end of a second will cause the storage register to become a counter, under DIACU control, to simulate the spacecraft time input and allow the DIACU to continue to maintain a time reference for the OCS. The ADC may read the spacecraft time storage buffer and the DIACU millisecond counter at any time.

The DIACU continuously compares the spacecraft time and the millisecond counter with a programable reference time sent by the ADC and stored in a 38-bit DIACU time monitor register. Upon comparison, the DIACU sets a bit in its interrupt status register. If the spacecraft time fails to function correctly for a period of more than 1 second the DIACU automatically switches over to an internal counter to provide a backup for spacecraft time.

All of the above operations are performed via the DI/O operated via 8 bit bytes. Two independent power supplies are contained in the DIACU. One is used only in the "Operating" power state and has circuitry identical to power conditioners used throughout the system for providing logic power. The other power supply in the DIACU is always on when DC power is supplied to the OCS. This is the Standby Power conditioner. It provides power for the DIACU "wake up" and time reference logic, and for the CADU discrete indicators.

The "wake up" circuitry senses certain signal inputs to the DIACU that require the OCS to leave the Standby power state and go to the Operating state. Wake-up is initiated by a time monitor match occurring, a CADU ALERT/STANDBY switch closure, or receipt of ACE-S/C Uplink or Up Data Link inputs. It turns on DIACU "Operating" power and performs turn-on of the ADC. The DIACU then issues an external interrupt signal to the ADC. The ADC, upon detecting this interrupt, commands the DIACU to transfer the contents of the DIACU interrupt status register to it. The ADC interrogates the interrupt status to determine what caused the interrupt and then resets the interrupt status register. Bit assignments are as follows:

0) Time Monitor Match
1) CADU Pushbutton Interrupt
2) Watchdog
3) ACE-S/C Updata Input
4) Spacecraft Uplink (Command Receiver) Input
5) Downlink Data Word Accepted
6) CADU Alert/Standby Pushbutton Switch Closed
7) Power-up Reset

Any non-zero condition in the status register causes an external interrupt to the ADC.

The DIACU provides power control outputs to the CADU and to the remote units of the OCS over a power control bus. This bus contains seven lines that carry a code to selectively turn on up to thirty-five power conditioning modules by combinations of power on four of the seven lines. The bus also contains a +5 volt DC line to power the sensing logic, a ground return line, and a master power disable line that turns off all units connected to the bus. Control of the signals on the seven code-output lines is provided by one-byte commands on the computer I/O channel.

The DIACU controls and provides power to the incandescent indicators on the CADU. Twenty-three of these indicators are controlled on or off by computer commands to a 24-bit indicator control register in the DIACU. Power circuits for these indicators and for the "Standby" indicator in the CADU are energized when the system in in either the standby or operating state.

The 1 pps signal from the spacecraft time interface causes the "watchdog" bit to be set in the DIACU status register. The ADC will then reset this bit. If a second 1 pps signal is received while the watchdog bit is set, the DIACU turns on the OCS No Go indicator on the CADU and forces the OCS to the standby state by sending a signal over the master power disable line of the power control bus. Loss of DIACU power will also cause the master power disable signal to be sent.

Two circuit types were considered for implementing the DIACU logic. The first was medium scale integration logic circuits (MSI). This approach had the advantages of lowering package count and reducing the printed circuit board layout complexity.

The second approach and the one which was selected was the use of low power integrated circuits. Their primary advantage was in lowering the logic circuit power requirements by a factor of almost ten. Their second advantage was in providing for more than one vendor.

Two methods of providing the system timing function were considered. The first was the inclusion in the DIACU of a multiplicity of hardware timing registers which could be set with a programmed delay at the end of which the computer would be signaled. Each timer would have added approximately five percent to the DIACU size and power requirements with a minimum of four timers being considered practical.

The approach selected here was the inclusion of one time match register which compared a programmed time value with the Spacecraft Time Reference and interrupts the central computer when a match occurs. Computer programming provides the means of selecting the proper time value to be set for this comparison. This approach not only saves hardware but also provides for a virtually unlimited number of system timers through appropriate software.

Where possible, one printed circuit layout card was made to do several jobs, thus reducing total engineering time for the unit. This technique was used in ACE UPLINK/UP-DATA LINK circuits, SPACECRAFT TIME interfaces, and the DUAL BI-PHASE REGISTERS.

Several problems were encountered in the development of this unit. Most important was the lack of a definition set of documentation covering the functioning of the IBM 4 Pi I/O channel. In particular, no information could be located to discribe the channel operation in response to errors at the interface. Thus the diagnostic equipment provided by the IBM system control panel could not be used effectively. The meaning of internal channel status indications was not fully described, so that little could be learned about the external hardware from the documentation.

A useful computer feature which was not provided was a means of forcing a software or hardware loop with a system unit as a response to error condition or an external signal.

A second problem occurred in wiring the baseplate connection in the DIACU. When the wiring passed the 50% complete point practically no room remained for soldering the wires to the pins or for the wires themselves. A successful attack on this problem requires an approach not normally used on short development projects. The more desirable approach would be as follows:

First, all circuit design must be complete before printed circuit board layout begins. Then optimum grouping of logic functions to make up individual boards to provide for minimum interfaces between boards. Next, input/output pins on these boards should be assigned such that the baseplate wiring is simplified and minimized. Finally, a mother board should be layed out to accommodate the necessary wiring. It is expected that several iterations of this last step may be required.

The importance of pre-testing circuits should be emphasized. Changing circuits in an airborne package after assembly is most difficult and time consuming. In addition, these changes frequently have damaging effects on the complex and somewhat fragile printed circuit boards. The more serious consideration was given during board design to withstanding airborne environment and less to withstanding the rigors of checkout on a development item. As a result, effort should be expended to reduce the strain of checkout on a board. Other measures could be taken to accomplish this, e.g., the addition of test points at the board edge would reduce the number of times the board needed to be removed from the chassis.

Another problem encountered was a severe undershoot on clock signals to binary elements. Voltage undershoot of more than 0.5 volt would result in erroneous changes of state for these binary elements. It was found that this problem could be eliminated by properly damping the clock signal line with the addition of from 30 to 170 ohms in series with the signal bias. More nearly optimum layout of baseplate wiring as mentioned above would also go a long way towards eliminating this problem without resorting to the damping resistors.

The DIACU weighs 19 lbs 9 ounces and requires a standby power of 42.5 and an alert power of 56.6 watts. The volume is 418 cubic inches.

E. POWER CONDITIONING/DATA CONTROL MODULE

Figure 8 shows a photograph of a PC/DCM. This module contains the data control module (DCM) circuitry necessary to interface with the data bus and the power conditioning circuitry (PC) necessary to convert the raw 28 volt spacecraft voltage to the required logic voltages. There are five of these standard PC/DCM modules in the OCS. They are interchangeable for purposes of maintainability. One of the five is a spare. Each PC/DCM weighs 6.9 lbs and is 170.5 cubic inches in volume. Its power level is included in the user module it supplys.

The PC/DCM will be discussed in two phases, data control and power conditioning

The data interface between the DIACU and the remote units is accomplished through two independent but identical transmission systems: A block diagram is shown in Figure 9. Each of these transmission systems consists of a common program data bus and a common response data bus. Both transmission systems may operate concurrently, resulting in a transmission bandwidth of twice that of a single system. This concurrent operation is utilized when providing numerical stimulus and measurements simultaneously. If one transmission system fails, the potential transmission bandwidth is reduced but the system will continue to operate. The software is designed to assure that the two transmission systems do not access the same remote unit at the same time.

Each remote unit is provided with data control logic and dual receiver transmitters (a separate receiver/transmitter for each transmission system) contained in a Power Conditioning and Data Control Module (PC/DCM). A block diagram of the data control section of the PC/DCM is shown in Figure 9 . The data control section receives biphase squarewave data on either of the common program data busses, converts the biphase signal to unit logic levels, recognizes the unit address, then shifts the data following the unit address into a holding register. The data control section of the PC/DCM provides capability to scan out the data contained in the holding register and transmit this data over the common response data bus of the same transmission system that the program data was received on. The Measurement Unit utilizes this response transmission capability of the PC/DCM to transmit measurement

FIGURE 8 - POWER CONDITIONING AND DATA CONTROL MODULE, COVER REMOVED

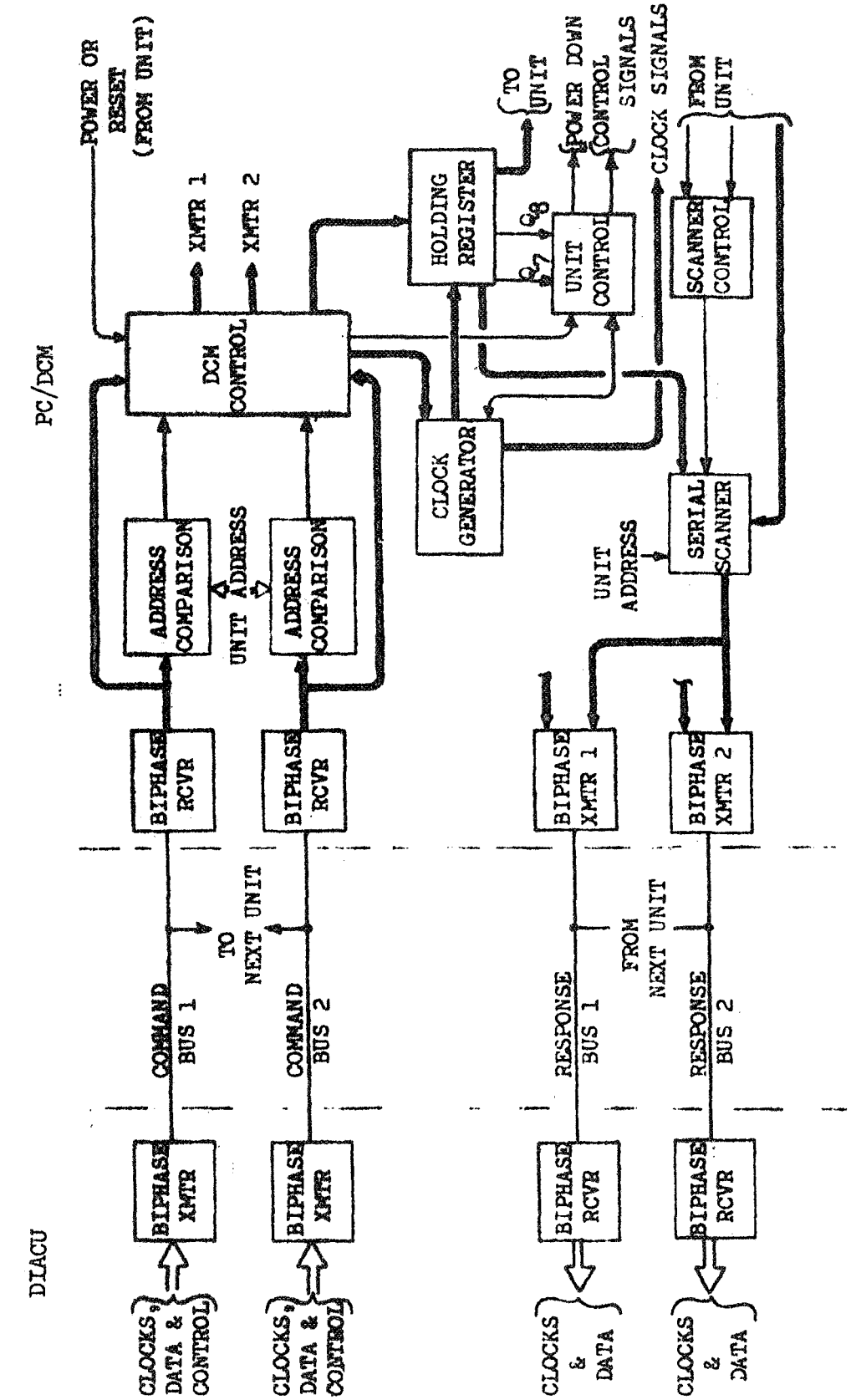


FIGURE 9 - DATA CONTROL SECTION OF PC/DCM

data through the DIACU to the ADC. The DIACU utilizes the dual transmitter/receiver portion of the PC/DCM but provides its own data holding registers for input and output.

The data control section of the PC/DCM in each remote unit allows each remote unit to be programmed from the ADC, via the DIACU and the computer-selected common program data bus. 24-bit data words are utilized for this programming. Of the 24 bits in the program data words, the first 6 bits in the data stream denote the remote unit address. For example, a binary code of 000111 in the first 6 bit positions of the data word designates the Stimulus Generator Unit. The seventh bit in the data word is assigned for control of unit power. When false (binary 0), bit 7 causes the PC/DCM to remove power from the addressed unit. The remaining 17 bits of the data word are used for programming the addressed unit.

Some remote units require more than 17 bits of data for complete programming. These units provide sub-registers and sub-register address decoding, so that multiple word groups received by the data control holding register can be transferred to the units.

The biphase receivers present a sufficiently high impedance that up to 30 PC/DCM's may be attached to the common data busses. The busses are twisted shielded pair cables with controlled impedances and are terminated with the cable characteristic impedance. The biphase receivers accept data from the common data busses through isolation transformers.

The biphase transmitters are capable of driving up to 300 feet of cable with up to 30 PC/DCM receivers distributed along the data buses. Only one transmitter will be active on a bus at any one time but the inadvertent activation of more than one transmitter on a bus at a time will not cause damage. The transmitters present biphase data to the common response data busses through isolation transformers.

Transmission on the data busses is at a one-megahertz bit rate, clocked by the DIACU. Thirty-one bits are actually transmitted to transmit a 24-program data word. The last seven bits of the program data word transmission are "dummy" bits, used to clock the 24-bit response word transmission which is delayed from the program data transmission by the six bit counts necessary for the addressed unit to recognize its address.

The data holding register of the PC/DCM data control section retains the 18 bits following the unit address until reprogrammed by another data message. Seventeen of these bits are available to the user unit to provide control and data for the functional operation of the unit. The holding register interface with the user unit is the Q_n and $\overline{Q}_n$ output of each register bit. These interface signals are capable of driving up to 40 low-power logic loads.

The response data scanner allows, under clock count control, the serialization of either the program data loaded in the data holding register or response data from the user unit data register, depending on the state of bit 8. The response data scanner interface with the user unit is the true (binary 1) output of 16 user unit data register stages.

Unit address patching is achieved by hardwiring at a connector, external to the PC/DCM. This external wiring of the unit address is used to allow identical PC/DCM's in all usages. The 6-bit hardwire address is compared with the first six bits of each transmitted program data word. A comparison allows the following 18 bits to be shifted into the holding register. The unit address, the power bit and the control bit (bit 8) are always transmitted back to the DIACU in front of the 16 bits scanned from the data holding register or from the user unit data register as described above. This allows the ADC to verify that the unit selection was correct and that the unit was properly programmed.

The remote group of the OCS hardware is made up of four types of units: Stimulus Generator Unit, Stimulus Switching Unit, Measurement Switching Unit, and Measurement Unit. As previously noted, up to 30 such units, in any mix, can be attached to the transmission systems. In fact, 30 units could be attached to each transmission system, for a total of 60 remote units, provided transmission system redundancy is not required. The OCS development system, however, provides only one of each type of remote unit and provides software for use of the transmission systems redundantly.

As described in the above section, each of the remote units utilizes a PC/DCM to provide power conditioning and interface with the transmission systems. The PC/DCM's are separately packaged and mounted adjacent to their user units in the development system. The package is easily attached or "removed" from a spacecraft coldplate.

The next few paragraphs document developmental results.

The data transmission employs redundant Command and Response databuses. These buses are transformer isolated and use a biphase signal transmission scheme to allow clock reconstruction, in addition to data recovery, thus making the redundant transmission system only a four twisted pair interface. The Digital Test Set transmission line, RG-108, attenuated the biphase signal considerably. Therefore, an investigation was made of possible alternate cables. A cable, Microdot 202-3934, appeared to have a much wider bandwidth, although increased characteristic impedance -- 160 ohms versus 78 ohms.

Test results using a 2 MHz squarewave signal indicated minimal signal attenuation with this cable. In addition, this cable was considerably lighter in weight giving it an additional advantage for a spaceborne application.

The biphase transmitter and receiver designs from the Digital Test Set were evaluated in terms of present airborne packaging trends. It was decided that new designs conducive to this trend, but using integrated circuits (flatpack and dual-inline packages) would be developed. Initial development testing used in-house transformer designs; however, a vendor, Contemporary Electronics Inc., of St. Louis Park, Minnesota, was found to employ similar hardware in the manufacture of a customer-special series of transformers. Subsequent consultation with them resulted in the decision to buy.

The Digital Test Set receiver design had a disadvantage in that it required two special voltages which required additional DC-DC conversion. New developments in the digital line receiver field, however, presented an alternative. National Semiconductor had developed a dual line receiver which required only +5 VDC logic power and provided better common mode rejection than the A710 Fairchild Comparator. Test data with a sample unit resulted in selection of this component for the receiver design. Subsequent use was also made of this component in the 4 Pi/EP interface control unit.

Breadboard circuits of both the transmitter and receiver designs were "patched" using special integrated circuit breadboarding fixtures and the in-house transformers tests were then conducted using the new transmission line for the data path between transmitter and receiver. Initial designs to use low-power TTL logic in certain areas of the transmitter

design were not feasible. Packaging of the resultant designs dictated two transmitters and two receivers on a single OCS printed circuit board (PCB). This allows use of this card also in the DIACU. This was accomplished without difficulty.

Use of redundant command buses also dictated use of two address decoders. The decoder design followed closely that of the Digital Test Set except for those changes dictated by use of TTL components. Both circuits were packaged on a single OCS PCB.

Since it is a function of the computer program to prevent addressing of the same Remote Unit over both Command bases, the redundancy was not carried beyond the address decoder. This required gating of the clock signals from either receiver one or two to the clock pulse generator; likewise for data to the storage register and likewise for the End of Transmission (EOT) signals for clock pulse generator reset.

The clock pulse generator and above gating circuitry is mounted on one card and the storage register and data scanner on another thus making a total of four cards to provide the data control requirement.

In addition to the data control provisions already described, the PC/DCM's each contain a power conditioner of the DC to DC converter type. A block diagram of this conditioner is shown in Figure 10. These power conditioners are enabled by the selective power enable circuit which originates in the DIACU. They provide stable output power to the OCS remote units from a prime DC power source contained in the right-hand bay of the support equipment cabinet. The "Type A" conditioners provide 5.25 ± 0.5 VDC at 5 amperes maximum and ± 20 ± 2 VDC at 600 milliamperes maximum. Where other voltages are required by the various user units, they are either derived from the above voltages through series regulator circuits or are provided by other conditioners contained within the units. The power conditioning modules supply floating outputs.

A coincidence of four logic signals on the seven "turn-on" wires of the power control bus causes PC/DCM power to turn on. Power "turn-off" is caused by either a zero on bit 7 of a program data word accepted by the PC/DCM or by a command on the master power disable line of the power control bus. To provide an initializing signal for the logic of the OCS user unit, the power conditioner of the PC/DCM provides a ground signal for a minimum of 100 microseconds to the user unit each time the power is turned on.

The Type A design also contains an undervoltage sensing circuit and a logic reset circuit.

The Type B power supply design provides the ±55 VDC power for the SGU output amplifier. Since it employed the same design approach as the Type A, LC filters were also employed on its outputs.

That part of the power control circuitry contained in the Type A and CADU power supplies is a combination solid-state and relay circuit. The relays are TO-5 packaged Teledyne latching units thus allowing the DIACU interface to be a pulsed operation. Actual power supply interface with the DIACU consists of 6 wires: power, power common and 4 control lines. There are 7 control lines originating at the DIACU but a 4 or 7 code is provided to accommodate up to 35 units (design requirement was 30). An SH2001 hybrid driver which is logic level signal compatible but which will provide the current required by two relay coils was selected as the interfacing unit. It has 4 logic-level signal inputs which were connected to the four control lines while its power and common leads were connected to power and common lines.

The OCS required the following power supplies:

a) Type a - Logic Power +5.25 ±0.5 VDC
+20.0 ±2.0 VDC
-20.0 ±2.0 VDC

b) Type B - ±55 VDC ±2 volts

c) Discrete - +28.0 ±4.0 VDC
+12.0 ±5%
+ 6.0 ±5%

d) DIACU Standby/Indicator +5.0 ±0.5 VDC
+15.0 ±2.0 VDC

e) CADU Type A +5.25 ±0.5 VDC
(±20 VDC available, not used)

Output transformer design was found to have an effect upon regulator switching spikes in the output. However, the greater effect was found to be caused by the recovery times of the rectifiers. Breadboarding involving both transformer designs and various rectifiers provided an optimum approach. Since off-the-shelf rectifiers were being used this was a compromise.

Some investigation was conducted into the use of various noise suppression techniques including ferrite beads. Significant changes were not observed on the breadboard unit. Feed-through LC filtering was provided on both the 28 VDC input and return lines and on the output voltage lines.

The design of all power supplies incorporates three basic sections. First is a preregulator which reduces the raw 28 VDC input voltage to a constant +19 VDC voltage. This regulated DC voltage drives the second section, the DC to DC converter which provides transformer isolation between the input power source and the OCS unit. The output DC voltages are determined by the preregulated input voltage and the turns ratio of the converter transformer reduced by internal losses in the supply. Since the load on these supplies is relatively constant these internal losses can be accounted for in the transformer design and the appropriate DC output provided.

The third section consists of rectification and filtering to provide ripple and noise reduction.

As a result of some of the problems identified during Digital Test Set design, development effort was expended in the following areas: output transformer design, diode recovery time versus noise in outputs, use of ground planes, use of noise suppression networks within supply, secondary regulation versus primary regulation and packaging.

Several power supply designs with the goal of standardizing the supply were considered.

Preregulation was chosen as the approach for two reasons. The first reason was that logic power is essentially constant. The second reason for the preregulator approach was that remote control of the power supply ON/OFF state provided minimal power drain in the OFF state as a byproduct.

The Type A power supply was used in the PC/DCM and DIACU units. During debug of the PC/DCM units it was observed that the noise level on the output voltage buses (no load to full load) was greater than anticipated. Investigation of the problem indicated most of the noise was being internally generated. Additional LC filtering was added on each output to reduce this noise to within expected levels. Even though this kind of LC suppression is effective, future power supply design should approach suppression of the noise source as mentioned previously rather than the noise itself.

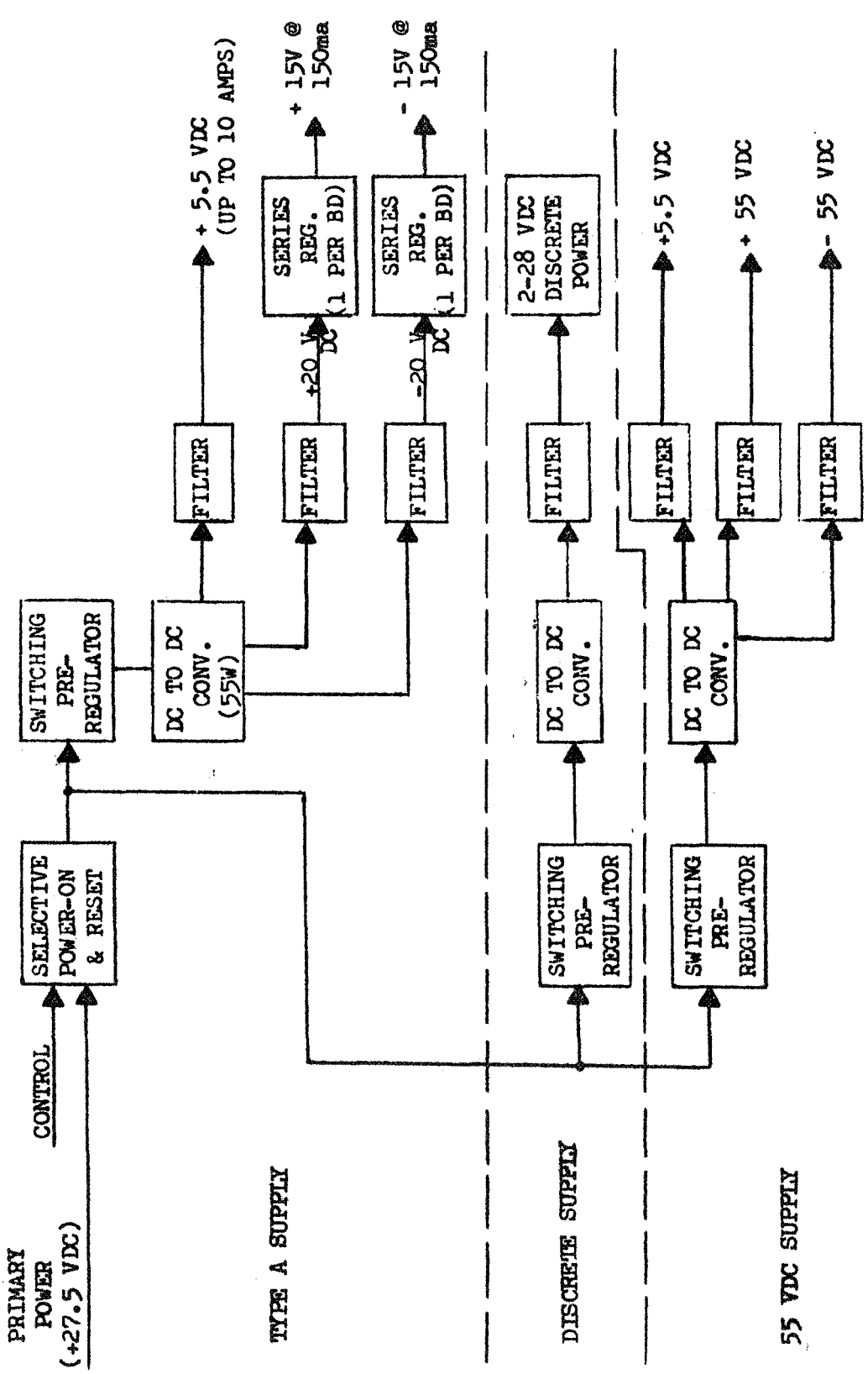


FIGURE 10- POWER CONDITIONING BLOCK DIAGRAM

F. STIMULUS GENERATOR UNIT (SGU)

This unit provides a programmable function generator capable, under computer control, of generating any of the stimuli listed in Table I. The unit is packaged in a case designed for easy attachment or removal from a spacecraft coldplate in the same manner as provided for the DIACU, the PC/DCM's, and all other remote units of the OCS. A picture of the SGU is shown in Figure 11. A block diagram of the SGU is shown in Figure 12. The unit weighs 19 lbs, 1 oz, requires 70 watts and uses 418 cubic inches.

The SGU is program controlled by data supplied to its PC/DCM data control receiver from either of the OCS Program Data Bus links. The control information is contained in a series of data words, each of which is temporarily stored in the PC/DCM holding register and then transferred to a holding register or counter in the SGU. There they remain stored until the holding register has been addressed with new data, the programmed count has been completed, or power is removed from the SGU. Four 24-bit words (each including a 6 bit address and a power bit) suffice to define any SGU output.

The SGU output is applied to an Analog Stimulus Bus upon a program data "Enable" command. The output remains on the Analog Stimulus Bus until a program data "Disable" command is received, or until another program data word or series of words defining a new output has been received. All AC signals are enabled through an interlock to assure that the programmed output will be applied to the stimulus bus as the signal output passes through the zero level. For single pulse or pulse train outputs, the stimulus bus is automatically clamped to SGU common upon completion of the programmed sequence.

Computer-generated functions (numerically-controlled waveforms) are accomplished by establishing a DC output and successively programming the amplitude and polarity of this output. An "Enable" command is sent by the computer as soon as the initial function control information has been transmitted. The computer then supplies the next amplitude and polarity command word to the PC/DCM holding register during the interval between SGU output steps. At the completion of each time interval the SGU enables a transfer of the PC/DCM holding register data to the amplitude and polarity holding register of the SGU. The SGU determines the time interval (based on program control) with an internal clock. A disable command is sent by the ADC upon completion of the computer-generated function.

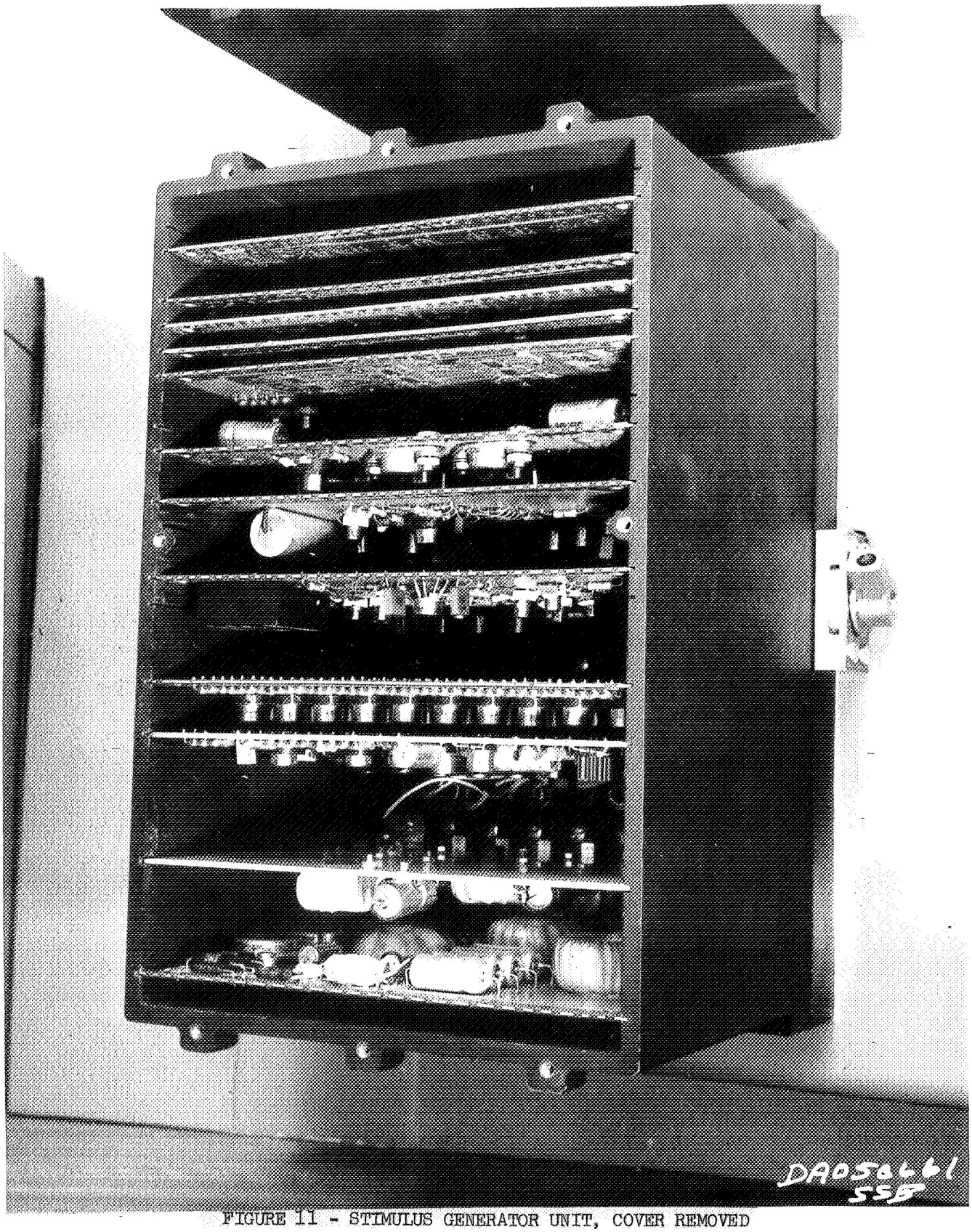


FIGURE 11 - STIMULUS GENERATOR UNIT, COVER REMOVED

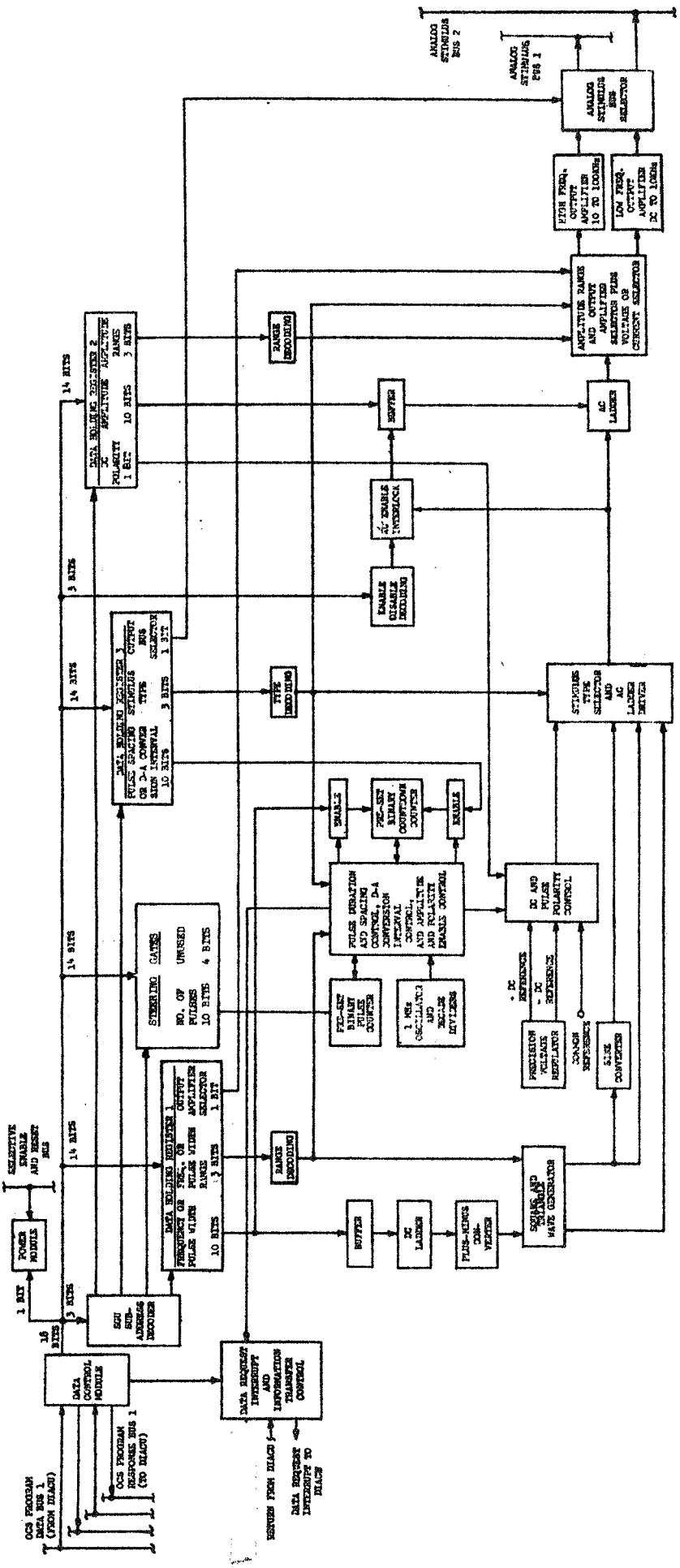


FIGURE 12 - SGU BLOCK DIAGRAM

TABLE I - OCS STIMULUS GENERATION CAPABILITY

STIMULUS TYPE	DURATION OR FREQUENCY RANGE	DURATION OR FREQUENCY TOLERANCE	AMPLITUDE RANGE	AMPLITUDE TOLERANCE	REMARKS
Sine, Square, and Triangle Waves	.1Hz to 10KHz in five ranges:		0 to 40V peak into 400 ohms minimum in three ranges:		Amplitude of all waveforms to be symmetrical about ground ± 1% of the programed peak to peak amplitude or ± 5mV, whichever is greater.
	.1Hz to 1Hz	± .01Hz			Maximum harmonic distortion for sine waves to be 1% from .1Hz to 20KHz, and 2% from 20KHz to 100KHz.
	1Hz to 10Hz	± (1% of programed value + .075Hz) or ± .10Hz maximum	0 to 1V peak	± (1% of programed value + 7.5mV) or ± 10mV maximum	
	10Hz to 100Hz	± (1% of programed value + .75Hz) or ± 1.0Hz maximum	1V to 10V peak	± (1% of programed value + 75mV) or ± 100mV maximum	Square wave rise and fall times to be as follows:
	100Hz to 1000Hz	± (1% of programed value + 7.5Hz) or ± 10.0Hz maximum	10V to 40V peak	± (1% of programed value + 300mV) or ± 400mV maximum	2 μsec. maximum rise time, 2 μsec. maximum fall time } .1Hz to 10KHz .5 μsec. maximum rise time, .5 μsec. maximum fall time } 10KHz to 100KHz
	1KHz to 10KHz	± (1% or progamed value + 75Hz) or ± 100.0Hz maximum			Amplitude of any square wave overshoot and ringing to be no more than 5% of the programed peak amplitude for any range.
	10KHz to 100KHz	± (1% or progamed value + 750Hz) or ± 1KHz maximum	0 to 10V peak into 75 ohms in two ranges: 0 to 1V peak	± (1% of programed value + 7.5mV) or ± 10 mV maximum	Maximum square wave droop to be no more than 1% of the programed peak amplitude for any range.
			1V to 10V peak	± (1% of programed value + 75mV) or ± 100mV maximum	Amplitude of any triangle wave overshoot to be no more than 5% of the programed peak amplitude for any range.
					Duration of square and triangle waveforms to be symmetrical about the half cycle points ± 1% of the full wave duration from .1Hz to 10KHz, and ± 2% from 10KHz to 100KHz.

TABLE I - (CONTINUED)

STIMULUS TYPE	DURATION OR FREQUENCY RANGE	DURATION OR FREQUENCY TOLERANCE	AMPLITUDE RANGE	AMPLITUDE TOLERANCE	REMARKS
DC Voltage	-	-	0 to 40V into 400 ohms minimum in three ranges: 0 to 1V	± (1% of programed value + 7.5mV) or ± 10mV maximum	Either positive or negative output may be commanded by program control.
			1V to 10V	± (1% of programed value + 75mV) or ± 100mV maximum	
			10V to 40V	± (1% of programed value + 300mV) or ± 400mV maximum	
DC Current	-	-	1mA to 250mA, into 160 ohms, in two ranges: 1mA to 100mA	Note 7 ± (2% of programed value + 1.5mA) or ± 2mA maximum	Voltage output capability from 0 to 40V maximum for any range. Either positive or negative output may be commanded by program control.
			100mA to 250mA	± (2% of programed value + 3.75mA) or ± 5mA maximum	

TABLE I - (CONTINUED)

STIMULUS TYPE	DURATION OR FREQUENCY RANGE	DURATION OR FREQUENCY TOLERANCE	AMPLITUDE RANGE	AMPLITUDE TOLERANCE	REMARKS
	5 μ sec. to 100 μ sec. in one range.	± (1% of programed duration + .2 μ sec.)	0 to 10V peak into 75 ohms in two ranges:		Amplitude of any overshoot and ringing to be no more than 5% of the programed peak amplitude for any range.
			0 to 1V peak	± (1% of programed value + 7.5mV) or ± 10mV maximum	Maximum droop to be no more than 1% of the programed peak amplitude for any range.
			1V to 10V peak	± (1% of programed value + 75mV) or ± 100mV maximum	Amplitude of any back swing and return swing to be no more than 5% of the programed peak amplitude for any range.
Voltage Pulse	100 μ sec. to 1 sec. in four ranges of one decade each	± (1% of programed duration + 2 μ sec.)	0 to 40V peak into 400 ohms minimum in three ranges: 0 to 1V peak	± (1% of programed value + 7.5mV) or ± 10 mV maximum	.5 μ sec. maximum rise time, .5 μ sec. maximum fall time } 5 u sec. to 100 usec 2 μ sec. maximum rise time, 2 μ sec. maximum fall time } 100 u sec. to 1 sec.
			1V to 10V peak	± (1% of programed value + 75mV) or ± 100mV maximum	In the pulse "Off" state, the voltage amplitude shall return to ground within ± 1% of the programed peak amplitude or ± 5mV, whichever is greater.
			10V to 40V peak	± (1% of programed value + 300mV) or ± 400mV maximum	Either positive or negative outputs may be commanded by program control. A total of up to 64 pulses may be generated in a single pulse train under program control.

TABLE I - (CONTINUED)

STIMULUS TYPE	DURATION OR FREQUENCY RANGE	DURATION OR FREQUENCY TOLERANCE	AMPLITUDE RANGE	AMPLITUDE TOLERANCE	REMARKS
Current Pulse	5 u sec. to 100 u sec. in one range	± (1% of programed duration + .2 u sec.)	1mA to 133mA into 75 ohms in two ranges: 1mA to 100mA	Note 7 ± (2% of programed value + 1.5mA) or ± 2mA maximum	Voltage output capability from 0 to 40V maximum for any range from 100 u sec. to 1 sec. Maximum rise time of 1 u sec. per volt measured acorss the amplifier sense resistor for 75 ohm loads. Maximum rise time 1 u sec. for the 1mA to 100mA range and 2 u sec. for the 100mA to 250mA range, measured across the amplifier sense resistor, for 160 ohm loads. All other pulse characteristic specitications to be the same as voltage pulse characteristics when measured acorss the amplifier sense resistor.
			100mA to 133mA	± (2% of programed value + 2mA) or ± 2.7mA maximum	
	100 u sec. to 1 sec. in four ranges of one decade each.	± (1% of programed duration + 2 u sec.)	1mA to 250mA into 160 ohms, in two ranges: 1mA to 100mA	Note 7 ± (2% of programed value + 1.5mA) or ± 2mA maximum	
			100mA to 250mA	± (2% of programed value + 3.75mA or ± 5mA maximum	
D/A Con-version	100 u sec. per step minimum	Note 5	-40V to +40V into 400 ohms minimum in three ranges: -1V to +1V	± (1% of programed value + 7.5mV) or ± 10mV maximum	Output voltage slew rate to be consistent with the rise time specified for voltage pulses. Amplitude of any overshoot and ringing to be no more than 5% of the programed step amplitude.
			-10V to +10V	± (1% of programed value + 75mV) or ± 100mV maximum	
			-40V to + 40V	± (1% of programed value + 300mV) or ± 400mV maximum	

TABLE I - (CONTINUED)

STIMULUS TYPE	DURATION OR FREQUENCY RANGE	DURATION OR FREQUENCY TOLERANCE	AMPLITUDE RANGE	AMPLITUDE TOLERANCE	REMARKS
Discretes	-	-	Discretes shall supply up to 150mA each at 2 to 28 VDC, with a maximum of four simultaneous discretes per level and a maximum of three levels per SSU. The maximum current output, however, shall be limited to 1 ampere per SSU.	± 5% of specified level from 2 to 28 VDC.	Applied directly from discrete voltage supplies in stimulus switching modules.

TABLE I - (CONTINUED)

NOTES:

1. All AC signals shall start at the zero voltage level ± 1% of the programed amplitude or ± 20mV, whichever is greater.

2. For pulse or square wave signals, the first pulse shall have the same duration and amplitude as all following pulses.

3. The maximum amplitude of a waveform will be defined as the amplitude exclusive of any overshoot, noise, or ripple.

4. Noise and ripple to be a maximum of 20mV peak to peak for any output of 1V peak or greater, and a maximum of 10mV peak to peak for any output of less than 1V peak.

5. The SGU shall be designed to perform direct D/A conversion at a conversion rate of 100 u sec. per step. Computer constraints will determine the actual system conversion rate.

6. The capability to provide a parallel 12 bit digital data stimulus channel to equipment under test shall be designed into the SSU. This interface will provide internal OCS logic levels.

7. The specified current amplitude accuracy will be degraded by approximately 1% for each load impedance increment of 1000 ohms. For load impedances less than 160 ohms, series impedance should be added external to the OCS to establish a total load of 160 ohms. The 10 KHz to 100 KHz output has a fixed load specification of 75 ohms and is not affected by provisions of Note 1.

Any program data word containing 27 (octal notation) in the first six bits will designate the SGU as the recipient of that data word. Any additional SGU's added to the OCS development system would require assignment of additional addresses. An SGU, PC/DCM, upon recognizing its address from the first 6 bits of the data word, will load the subsequent 18 bits of the data word into its holding register. The first bit loaded onto the register is the previously discussed power control bit. The next three bits contain sub-addressing information to designate the pulse counter or one of three 14-bit sections which made up the SGU data holding register. An "end of transmission" signal from the PC/DCM enables parallel transfer of data to the SGU counter or appropriate holding register section, unless there is an inhibit signal present. The inhibit signal will be present whenever the SGU is operating in the direct D-A conversion mode (converting computer-generated functions) and is counting the interval between one step and the next. This allows a word to be loaded into the PC/DCM for buffered storage until the SGU completes the step interval count and is ready for a new step in amplitude. Then the inhibit signal is removed, the data automatically transfers to the amplitude and polarity section of the SGU holding register, and a "Data Request" interrupt signal is sent from the SGU to the ADC on a separate line. This is the Data Request Interrupt signal. It is a "Priority" interrupt, in that is requires priority attention by the ADC to immediately generate the amplitude and polarity program data for the next SGU output.

The first 14-bit section of the SGU holding register, loaded by the sub-address 001 (binary notation), is decoded to select the computer-specified SGU signal output frequency or pulse width and either a high or low frequency output amplifier for the signal. The second 14-bit section of the holding register is loaded by sub-address 010 and is decoded by the SGU to select the polarity for DC outputs and the signal amplitude. Frequencies, pulse widths, and amplitudes are specified by 10-bit binary numbers and 3-bit range or exponent codes. The third 14-bit section of the holding register is loaded by sub-address 011 and is decoded to select the specified stimulus type, the spacing for pulse train outputs or the time interval between steps in direct D-A conversion, and the stimulus bus on which the output is to appear. The SGU is designed to accommodate two stimulus busses. Only one bus, however, is provided in the OCS development system.

Sub-address 100 loads a "number-of-pulses" counter. The data stored in this counter is decoded to select a specified number of pulses in a pulse-train output. Stimulus enable commands are decoded from a sub-address of 101 and disable commands are decoded from a 110 sub-address.

The PC/DCM provides read-back of SGU program data to the ADC to allow verification of the data in the holding register. An enable command is never issued to the SGU until the ADC has made this verification.

When more than one SGU is used in the OCS, it becomes necessary for the ADC to poll each SGU to determine which one has sent a "Data Request" interrupt. To provide for such multiple SGU operation, the SGU sends a Data Request Interrupt Status but back to the ADC through the normal data read-back capability of the PC/DCM when it receives a message with a sub-address of 111.

The analog stimulus bus is a twisted shielded twin-ax pair. The SGU output can be programmed to either of two such busses although only one is provided in the OCS development unit. Either of the two SGU output amplifiers can be switched to either stimulus bus output. An interlock is provided to prevent more than one SGU at a time applying an output to any one stimulus bus.

The SGU design was based on the circuit philosophy established with the stimulus unit in the Digital Test Set (DTS). New performance requirements for the OCS resulted in the addition of a zero-crossing detector enable circuit and a repetitive or sequenced pulse output circuit. The circuit philosophy is still based on the use of an integrator to generate the basic triangle and square wave function generator outputs. A D/A converter is used to develop scaled input voltages. These voltages are then applied to the integrator input and a specific feedback ratio selected to establish the desired frequency. The ramp output of the integrator is allowed to reach a specified peak value, at which point a comparator actuates input switching to reverse the direction of the ramp. The same switching action also provides the square wave output. Shaping networks are used to synthesize a piecewise linear approximation of a sine wave from the basic triangle. The program selected functions are applied to an AC amplitude -- scaling D/A converter, and then to the output amplifier.

Critical analysis of the 14 bit resolution provided in the DTS A/D converters showed that adequate resolution could be achieved with only 10 bits. Since significant size reduction was desired for the OCS, the 10 bit system was immediately adopted. This decision reduced the size of the holding registers and A/D converters to the 10 bit size while still providing resolution of one part per thousand. Similar size reductions were achieved by using state-of-the art integrated operational amplifiers in the integrator input circuits. As a result, the OCS utilized two TO-5 devices where the DTS had used two hybrid amplifiers occupying areas of several square inches each. An integrated current source was also used to replace the D/A voltage scaler, which previously had required an entire circuit card. Similarly, the DTS comparator was a discrete component design requiring an entire circuit card, and this design was replaced in the OCS with a single TO-5 integrated circuit comparator. The integrator itself was substantially reduced in size even though a hybrid amplifier was retained. This amplifier is less than half the size of the DTS integration amplifier. An integrated circuit TO-5 amplifier was actually used in breadboarding and functioned well within specifications to 28 KHz. Degradation from 20 KHz to 100 KHz in the triangle wave was, however, too extensive to permit use of the integrated circuit in the final design. Additional size reductions were achieved by using simplified inverted transistor switches to achieve analog switching with minimum voltage offsets. A holding register for programming the number of pulses in an output was eliminated by logic manipulation which permitted the counter itself to store the information.

After the final fabrication, the SGU was calibrated. The output capability was found to be generally consistent with the contract specifications. Some circuit card modifications were incorporated to effect design improvements or optimize overall system operation. Frequency, amplitude, distortion, and waveform fidelity were within contract specifications. Noise generated within the power conditioning circuits, however, coupled with the capacitance of the metal core circuit cards, resulting in a ringing frequency of approximately 2 MHz. Due to this noise, the metal core capacitance, and insufficient ground plane area, the rise time accuracy of the output waveforms was marginal.

Specific improvements in SGU performance could be achieved by judicious removal of metal core (and the resulting capacitance) from sensitive area. This would require developmental determination of the proper areas of sensitivity. Similarly, the output leads from the final drive stage of the output amplifier are relatively long and pass through a connector to permit heat sink mounting of the final stage transistors. The feedback loop must be closed through the same connector. Eliminating the connector and shortening these leads would improve the rise time considerably. It should be noted that the breadboard system was well within specification limits.

G. MEASUREMENT UNIT (MU)

The MU converts the analog measurement signals appearing on the analog measurement busses into a digital format for interpretation by the computer. The MU consists of a PC/DCM and signal conditioners, detectors, converters, and control logic. The MU is packaged similar to the other remote units described above. Figure 13 presents a block diagram of the unit and Figure 14 an actual photograph of the unit. The unit weighed 19 lbs 12 oz, required 418 cubic inches and uses an average of 42.9watts.

Provision is made for interfacing the MU with two measurement channels, either of which can be selected by the MU for inputs. A measurement channel consists of two measurement busses, bus A and bus B. A single channel can input to only one MU at a time, and in the OCS development system only one channel is actually provided.

The measurement conversion capability of the MU is presented in Table II. Analog measurement bus A is used for all voltage, frequency, time, serial digital data, and contact closure measurements. Bus B is used for input of the second signal when measurement of time interval or phase between two signals is required. Bus B is also used to input the clock signal on digital data inputs requiring clocked decoding.

The MU receives power from and is programmed by a PC/DCM. As in the other remote units, the first six bits of the program data words provide the addressing that causes the MU PC/DCM to accept program data from the ADC. The single MU provided in the OCS development system has the address 011011 (octal 33). Bit 7 of the program data word operates to power down this unit just as it does any other addressed remote unit. Bit 8 is used to cause the MU to either accept and transmit back the entire program data word to or transmit a measured result. Bit 9 is used for sub-addressing to control the parallel transfer of bits 10 through 24 of the program data word from the PC/DCM data holding register to either one of two holding registers in the MU.

The first 15-bit MU holding register (loaded by the presence of a 0) in bit 9 of the program data word) is decoded to select the amplitude range on bus B, the trigger level for bus B, and the time interval between repetitive voltage measurements.

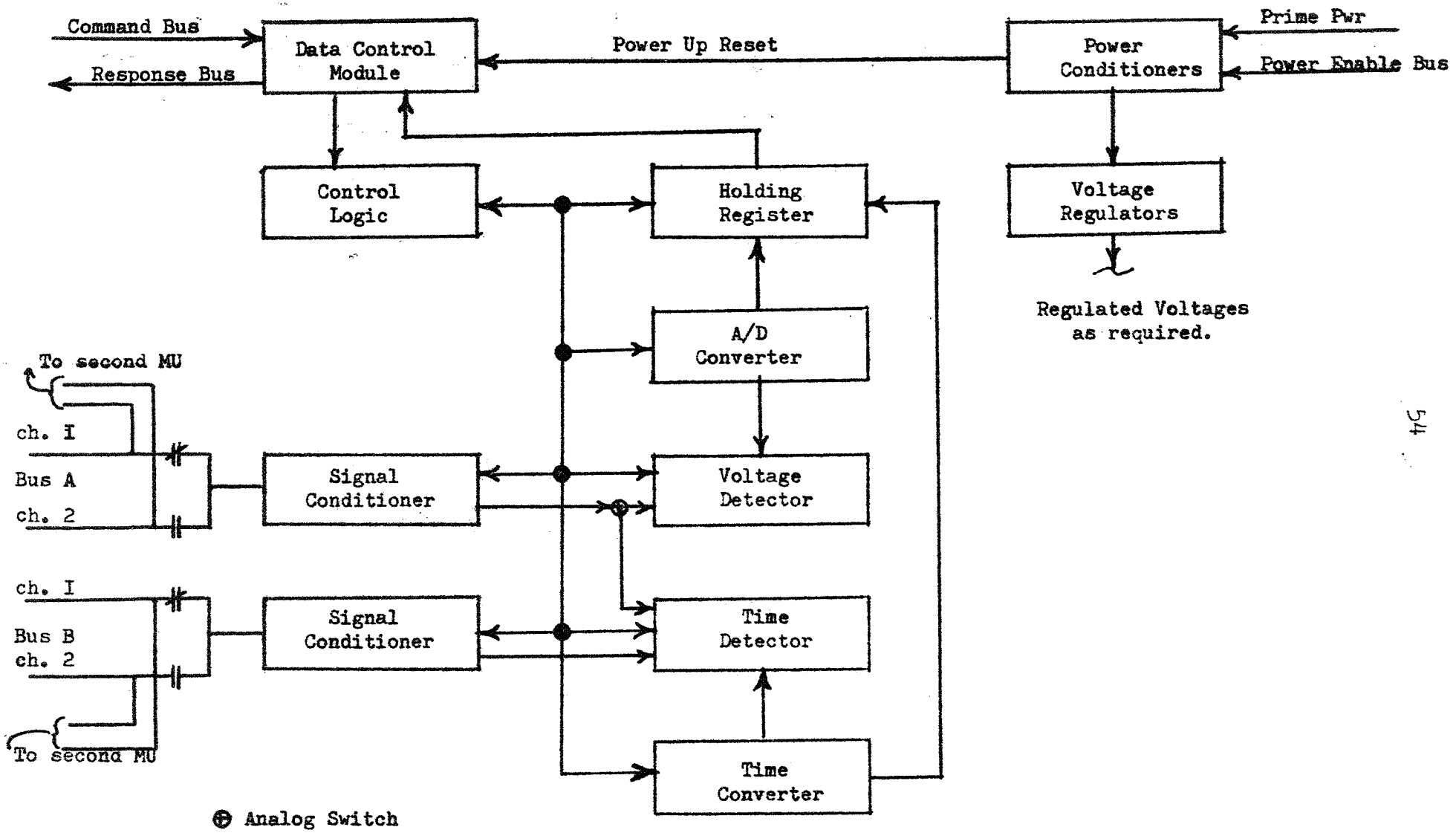


FIGURE 13 -MU BLOCK DIAGRAM

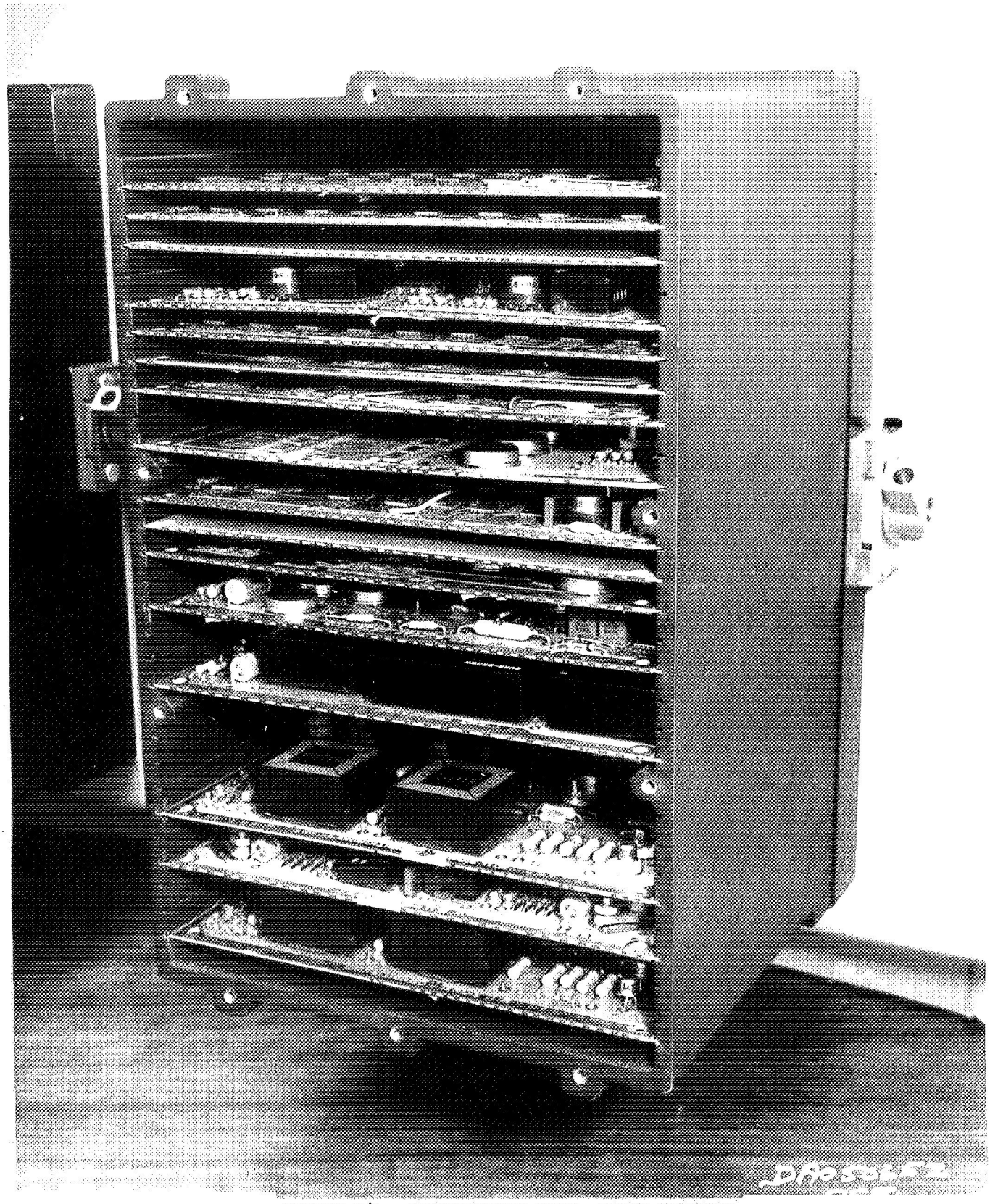


FIGURE 14 - MEASUREMENT UNIT, COVER REMOVED

TABLE II - OCS MEASUREMENT CAPABILITIES

MEASUREMENT TYPE	RANGE		ACCURACY	REMARKS
	VOLTAGE	FREQUENCY/DURATION		
DC Voltage (Bipolar)	10mV to 1V	-	± (1% of value + 2mV)	
	1V to 10V	-	± (1% of value + 20mV)	
	10V to 40V	-	± (1% of value + 200 mV)	
AC Voltage Peak (Sine, Square and Triangle)	50mV to 1V	0.1Hz to 10KHz	± (1% of value + 4mV)	
	1V to 10V		± (1% of value + 40mV)	
	10V to 40V		± (1% of value + 400mV)	
	50mV to 1V	10KHz to 100KHz	± (1.5% of value + 4mV)	
	1V to 10V		± (1.5% of value + 40mV)	
AC Voltage RMS (Sine)	50mV to 1V	10Hz to 50Hz	± (7.5% of value + 6mV)	
	1V to 10V		± (7.5% of value + 60mV)	
	10V to 40V		± (7.5% of value + 600mV)	
	50mV to 1V	50Hz to 10KHz	± (1.5% of value + 6mV)	
	1v to 10V		± (1.5% of value + 60mV)	
	10V to 40V		± (1.5% of value + 600mV)	
	50mV to 1V	10KHz to 100KHz	± (2% of value + 6mV)	
	1V to 10V		± (2% of value + 60mV)	

TABLE II - CONTINUED

MEASUREMENT TYPE	RANGE		ACCURACY	REMARKS
	VOLTAGE	FREQUENCY/DURATION		
Discrete (Bipolar)	2V to 32V	-	± 5% of value	
Contact Closure	-	Logic Decision	-	Discrete voltage provided by M.U. to unit under test.
Time Interval (Single or Dual Channel)	50mV to 10V peak Note 1	1 μ sec. to 10 μsec	± 0.1% of value or ± 0.1 μsec. whichever is greater	Time interval is defined as time between positive or negative start slope to positive or negative stop slope. Input must be symmetrical about signal common, or the low voltage state must not be removed from signal common by more than 10% of the peak voltage. Rise and fall time are assumed to be instantaneous.
	50mV to 10V peak	10 μsec. to 100 μsec.		
	50mV to 40V peak	100 μsec. to 10 min.		
Frequency	50mV to 40V peak	0.1Hz to 10KHz	± 0.1% of value or ± 0.1 μsec. whichever is greater	Input must be symmetrical about signal common, or the low voltage state must not be removed from signal common by more than 10% of the peak voltage. Rise and fall time are assumed to be instantaneous.
	50mV to 10V peak	10KHz to 100KHz		
Phase (Sine)	50mV to 40V peak	0° - 360°	± (1° + 0.2 μsec.)	Frequencies identical and voltages not more than 1 decade apart. Inputs symmetrical about signal common.
Pulse Code Modulation	-	-	-	Provide hardware to accept a 51.2 K.B.S. P.C.M. conditioned serial pulse train. Provide capability to select adjacent word groups (8 bits per word) up to 400 words from the pulse train and transfer them to the computer.

TABLE II (CONTINUED)

MEASUREMENT TYPE	RANGE		ACCURACY	REMARKS
	VOLTAGE	FREQUENCY/DURATION		
Frequency with DC Offset	-	0.1Hz - 100KHz	± 0.1% of value or ± 0.1 μsec. whichever is greater.	The ratio of signal p-p voltage to DC offset voltage must be equal to .5 or greater. Input signal amplitude must be 100 millivolts p-p minimum, and the maximum offset plus signal voltage must not exceed 40 volts.
Digital Data Type A, B, & C as defined in Note 4.	-	-	-	Note 4
Totalizing (Discrete number of pulses)	-	-	-	Maximum number of pulses is 10,000. M.U. timed out by the computer. Input amplitude from 100 millivolts peak to 40 volts peak. Input must be symmetrical about signal common, or the low voltage state must not be removed from signal common by more than 5% of the peak voltage.

Special Note: The MU accuracy is based upon the sum of measurement accuracy (% of input value) and of fixed offsets which are a function of range and not of value.

TABLE II CONTINUED

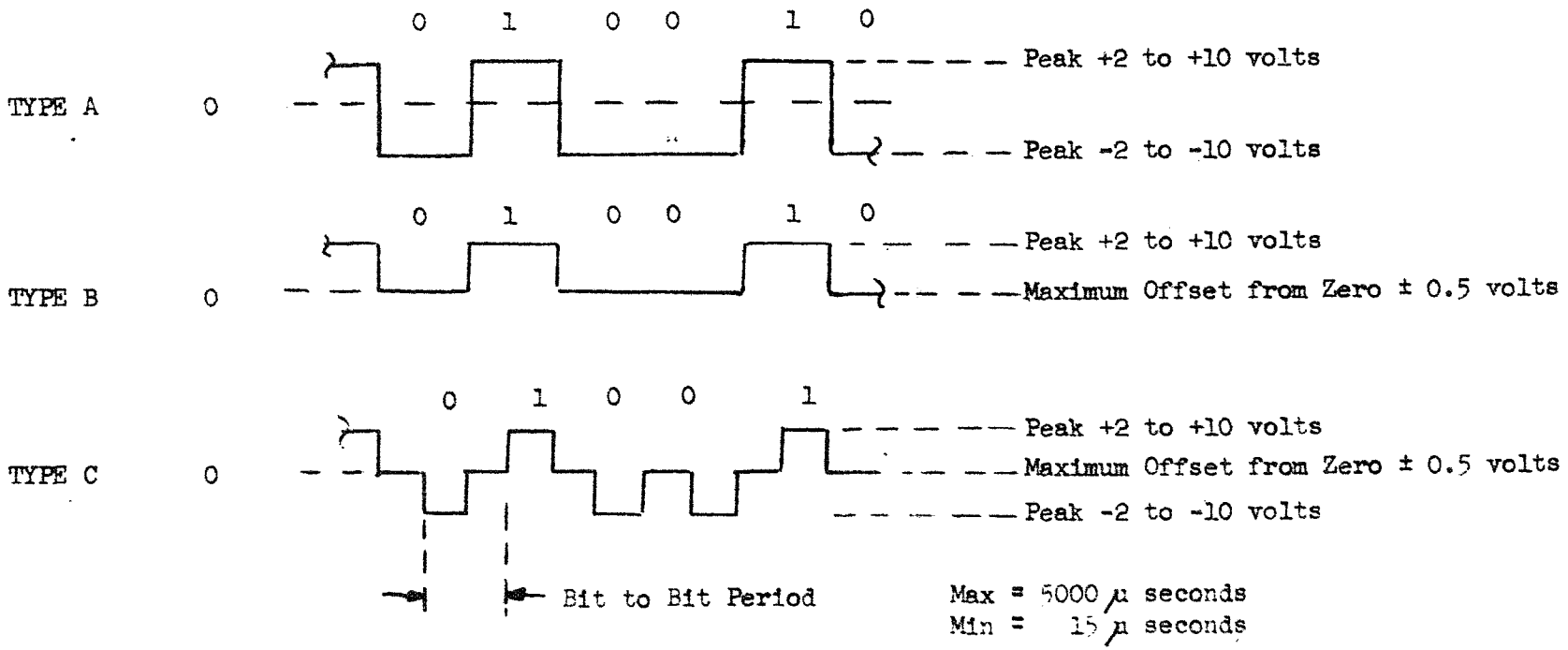
NOTES:

1. The Measurement Unit input impedance shall be a minimum of 2 megohms shunted by a maximum of 33 pico-farads, for frequencies below 10 KHz, a minimum of 200 K ohms shunted by a suitable capacitance to frequencies above 10 KHz and a minimum of 10K ohms shunted by a suitable capacitance for time intervals below 10 u sec.

2. The Measurement unit A/D conversion speed will be 100KHz. The time interval between MU controlled repetitive voltage measurements shall be 500 u sec. to 100 m sec., in 100 u sec. steps.

3. Commercial test equipment shall be used to prove the Measurement Unit accuracies.

4. Digital Signals Interface - Digital data inputs to OCS from the Unit Under Test shall utilize existing paths through switching modules. Circuitry within the OCS shall convert TYPE A and B non-return to zero (NRZ) and TYPE C return to zero (RZ) waveforms as shown below to OCS internal logic levels. Once converted to OCS internal logic levels the data shall be loaded into a register which shall be interrogated under computer control via the existing Data Control Module response converter. The Unit Under Test shall issue digital data only upon command from the OCS by use of a discrete command from the SSU. The software required for this digital measurement will consist of a special element to control and evaluate the digital data input.



The second 15-bit MU holding register (loaded by the presence of a "1" in bit 9 of the program data word) is decoded to select measurement frequency range, measurement channel, amplitude range on bus A, trigger level for bus A, and type of measurement. The data in this register also includes one bit that specifies whether a single measurement or repetitive measurements are to be taken. Another bit designates either the use of bus A only or the use of both bus A and bus B for the measurement.

All voltage, phase, frequency, and time measurements are signal conditioned and then routed to the appropriate converter or detector. Contact closure measurements are made by routing a 5 ma DC signal from the MU, over the measurement bus and through the MSU and the contacts to be checked, and detecting the presence or absence of the return.

Upon completion of a measurement conversion, the MU sends a "Data Ready" signal to the ADC (via the DIACU) on a separate line. This is the Data Ready Interrupt signal mentioned in the discussion of the DIACU. It informs the ADC that the measurement conversion is complete. The ADC responds to this interrupt by transmitting a program data word to the MU requesting transmittal of the 14-bit contents of the MU output data holding register which holds the converted measurement value. As previously noted, the eighth bit of this program data word provides the control that causes the MU to transmit the measurement value on the response data bus. Bit 9 of this response word will be "true" if the addressed MU had sent the Data Ready signal. This allows the ADC to determine which MU interrupted it if several MU's were operative in the system.

Bit 10 of the MU response word is used for contact closure measurements and to indicate a time interval counter overflow on time interval measurements. A "one" in this bit position indicates "contact open" on a contact closure measurement or that a time interval measurement has exceeded the measurement range.

The next paragraphs discuss measurement unit developmental results.

The signal conditioning function required a developmental high performance integrated circuit operational amplifier, where high performance requires high input impedance and wide bandwidth. Several vendor units were tested before the final unit was selected. The critical selection of this amplifier would be eliminated if the frequency range and/or input impedance specification could be reduced. The compensation and balance of the front end signal conditioning circuitry is quite critical due to the wide band requirements. If these

circuits are not tuned properly, a time constant mismatch and attendant spiking will produce erroneous results for peak measurements.

The RMS function of the MU was in addition to the DTS function so this presented a new design requirement. Accuracies of the squaring amplifiers tested were such that is was found necessary to insure that this amplifier was operating between half and full scale of output. This was accomplished by incorporating an additional pre-ranging and post-attenuation circuit. The RMS system proved to be a wise addition to the MU functions, since by definition it is not sensitive to noise spikes.

Several techniques were investigated for handling AC measurements with DC offset. Capacitor coupling was ruled out again because of wide frequency range problems. The final technique employed involves precharging two capacitors, one to the positive peak the other to the negative peak voltage, then their difference used to cancel the offset. This technique was used successfully for repetitive waveforms. The non-repetitive waveforms are handled by programming standard offset voltages which buck the offset, and in essence, set the trigger level.

The repetitive analog to digital sampling function is in addition to DTS requirements. By additional control logic the A/D converter operates repetitively and was tested satisfactorily to a 400μ sec sample rate.

The OCS measurement unit successfully met its design requirements for ten of its twelve measurement types while peak voltage and phase measurements were marginal in their accuracies.

While both of the modes could be noticeably improved in the present equipment by very precise balance and compensation of the signal conditioning circuitry, there are some basic difficulties which if overcome should rectify the accuracy problems in question, as well as improve the overall unit accuracy.

The first improvement that must be realized is a reduction in the converter noise output of the power supplies. This would permit a reduction in the hysteresis required in the delta-detector circuitry resulting in improved phase and time-interval measurement accuracies.

The second area to investigate is that of heat dissipating techniques with the target of eliminating the use of metal core printed wiring cards. This would significantly reduce the circuit capacity of the signal conditioning circuitry reducing the degree of difficulty for accurate compensation. This coupled with an improved unit ground system should result in "in spec" peak voltage measurements.

The control logic of the measurement unit should be modified to the extent that there is complete independence between modes of operation, that is, those modifiers that do not directly apply to a particular type of measurement should be permitted to be in "don't care" states; i.e., the frequency modifier should be permitted "don't care" status when making a totalizing measurement.

H. STIMULUS SWITCHING UNIT (SSU)

The stimulus signal interface between units under test and the SGU is provided by a Stimulus Switching Unit. The SSU requires a PC/DCM, identical to the PC/DCM's provided for the SGU and other remote OCS units, to provide power conditioning and programming. The SSU is packaged similar to the SGU. A block diagram of the unit is shown in Figure 15 and an actual photograph in Figure 16. The unit with its associated PC/DCM weighs 15 lbs and 10 oz, and requires 28.3 watts of power.

The SSU is programmed by the data holding register outputs of its PC/DCM. When the first six bits of the data word contain the SSU address (octal 66 for the single SSU provided in the OCS development unit) the SSU PC/DCM is selected. Bit 7 controls power on the SSU as it does for the SGU. Bit 8 is used to signify that either the data holding register is to be loaded and scanned out on the response bus or SSU switch address comparator self test bits are to be scanned out on the response bus. The 9th bit of the command word is used by the SSU to steer input data either into its switch selection register or into its "digital data holding" register. The next twelve bits are used to specify a switch point selection or to load the digital holding register.

The decoding technique used for switch point selection provides code spacing such that a single bit error or a single component failure in the PC/DCM holding register will not allow an incorrect switch point to be selected. Any other failure which causes an incorrect switch point to be selected will be detected by switch address comparators which compare the actual switch point selected against the switch point requested. In addition to this protection, a quad switch arrangement is employed so that a single relay contact failure will not result in closing an incorrect switch point.

The SSU of the OCS development unit provides 36 double-pole switches, for switching both signal and return of 36 stimulus points. Addressing capability is provided, however, for an expanded SSU of up to 144 switches.

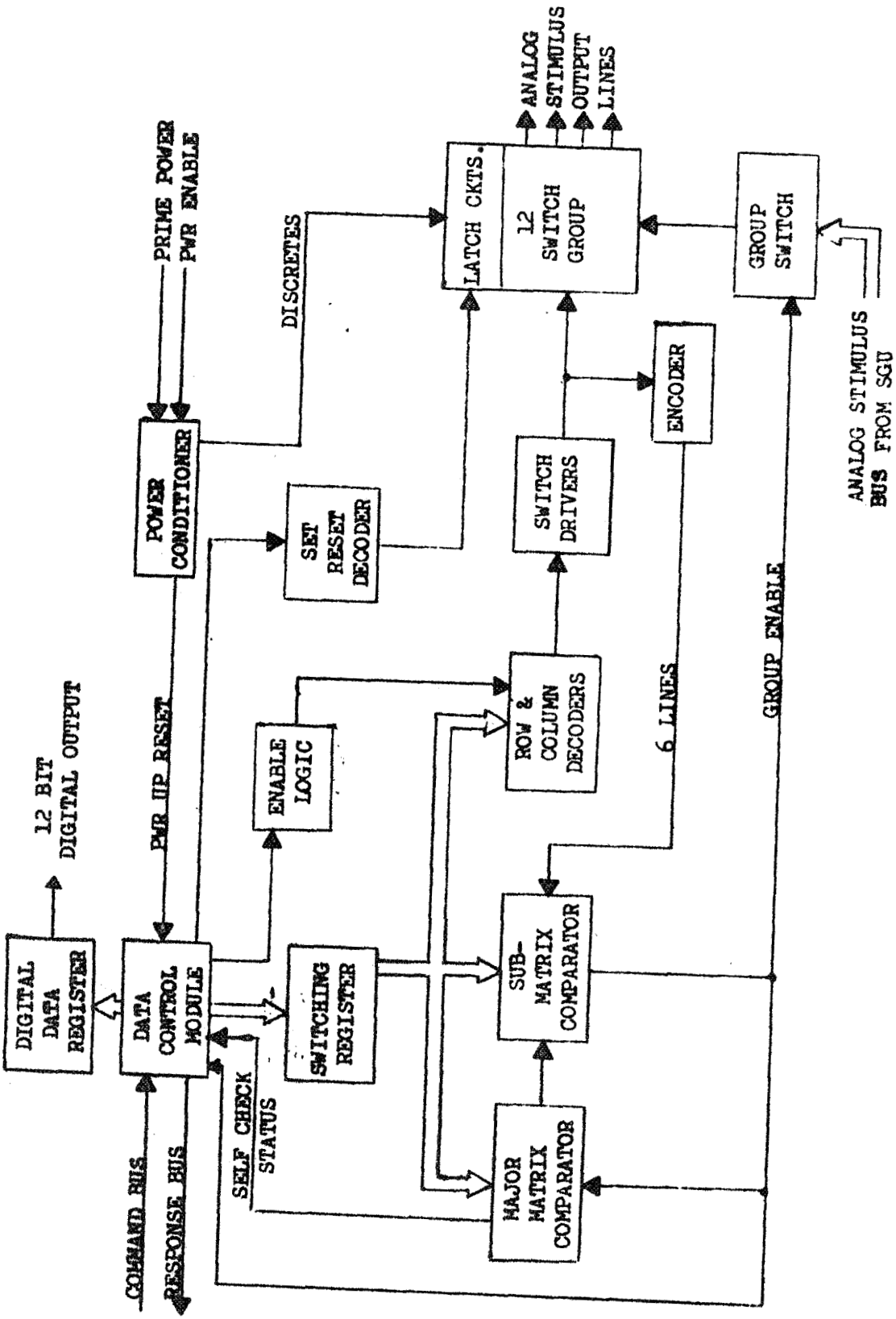


FIGURE 15 - SSU BLOCK DIAGRAM

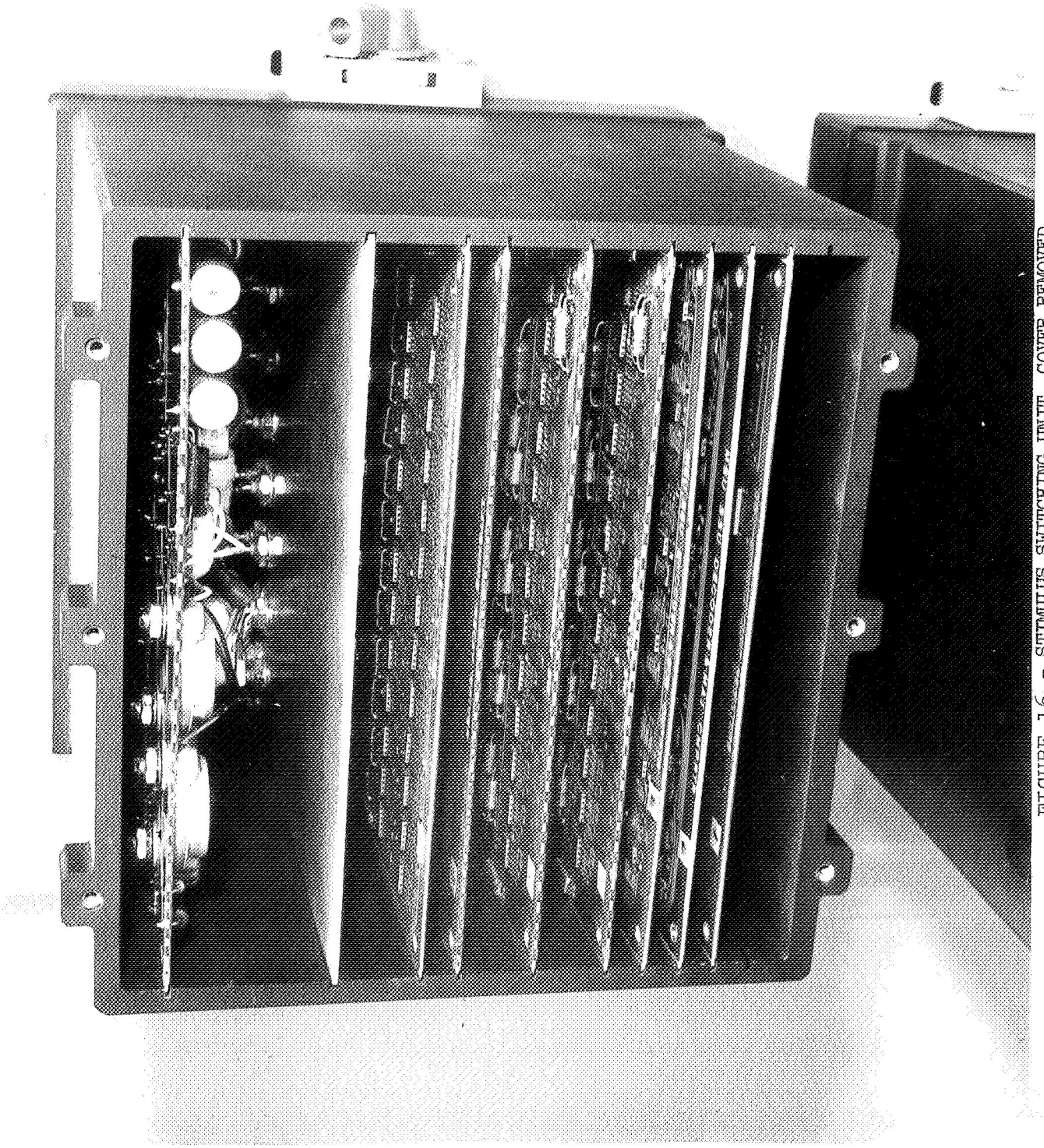


FIGURE 16 - STIMULUS SWITCHING UNIT, COVER REMOVED

Switch selection and control is in 2 x 6 submatrix groups of twelve switches. Three such submatrix groups are assembled into a 3 x 1 major matrix. A 6-bit submatrix code and a 6-bit major matrix code are decoded into six rows of 6 columns as shown in Figure 13. This figure also shows the code assignments as they would be expanded to a 144 switch point unit. A 12-bit row and column code will cause the selection of a specific switch within a specific submatrix (group of 12). The switch driver output of the switch thus selected is then encoded into a 6-bit code and compared with the 6-bit submatrix address contained in the data holding register. The 6-bit major matrix code is compared against hardwired codes to develop major row and column lines. These row and column signals are combined with the output of the submatrix comparator to allow enabling of the appropriate submatrix analog input relay if all comparisons are true. The analog input switch will pass the programmed analog stimulus from the analog stimulus bus to the selected stimulus switch and on to the unit under test stimulus point.

Of each 36 switches in a SSU, 12 are latching type. These can be made accessible to either the stimulus bus from the SGU or to any one of three discrete voltage busses internal to the SSU and powered by a special SSU internal power conditioner. The patching for this purpose is accomplished at a patch connector external to the SSU. Voltages available from the SSU discrete voltage busses are: 28 $\pm$ 4 VDC at a 600 mA max., 5 VDC $\pm$ 5% regulated at 150 mA max., and 12 VDC $\pm$ 5% regulated at 150 mA max. Bit 22 of the program data word is used to program a latch of a latching switch. Bit 23 is used to reset a latch.

The PC/DCM provides read-back of its program data. The three group enable signals formed by the address comparators are used to generate a self-check status indication. This signal is inserted into the twenty-fourth bit position of the data word during the period when the data holding register is being scanned back to the computer. Sending a "one" to the computer indicates a successful programming of the SSU.

When a "zero" is sent by the computer in bit 8 of the program data word, the individual comparator outputs are presented to the response data scanner so that they may be read by the computer for SSU fault isolation purposes. There are three comparator outputs for each set of 36 switch points (a maximum of 12 outputs for a 144 switch-point SSU). In the 36 switch SSU provided in the development system the 9 unused comparator output bits are hardwired "true".

In addition to the analog stimulus and discrete voltage switching provided, the SSU provides a parallel 12-bit digital data output channel. This feature is implemented by a 12-bit register that is loaded when a "one" is contained in the ninth bit of the program data word. The data is held in this register, providing a 12-bit 5 VDC parallel digital output over the SSU digital data channel, until the register is reprogrammed. A return line to SSU ground is provided for this channel.

No significant developmental problems were encountered on this unit as it was primarily a repackaging of the DTS design. The SSU met all of its design goals without exception.

A trade off of solid state versus relay switching was performed and the results indicated that because of the current flow requirement through the switch it was necessary to use relays. The SSU is implemented with microminiature relay switches.

The back plane wiring utilizes shielded wire for switch input/output. This caused difficulty in fabrication. If this could be eliminated not only would fabrication be facilitated, but a significant weight savings would be realized.

I. MEASUREMENT SWITCHING UNIT (MSU)

The MSU provides the signal interface between units under test and the OCS Measurement Unit. It is a program controlled switching unit, similar in most respects to the SSU but using solid-state switching devices rather than relays. Packaging is similar to that provided for the SSU and other remote units. As in the SSU, switch selection and control is 2 x 6 submatrix groups of twelve switches each. Switch selection decoding, encoding, comparison, and generation of self-check signals is accomplished exactly the same as in the SSU. The MSU contains switching for 72 switch points. As in the SSU, addressing capability is provided for up to 144 switch points. The same failure protection and detection provisions are contained in the MSU as are provided in the SSU. A photograph of the MSU is shown in Figure 17. The unit with its associated PC/DCM weighs 21 lbs 7 oz, and requires 28.3 watts.

The MSU is addressed by octal 35 appearing in the first six bits of a program data word on the program data bus. As in the other remote units, the seventh bit controls turn-off of the MSU PC/DCM power conditioner. The eighth bit is used to control the makeup of the MSU response word. If bit 8 is a "1", the data holding register is loaded and scanned back out on the response data bus (with bit 24 containing self-test status as described for the SSU).

If bit 8 is a "0", the 6 address comparator outputs (one for each 12-switch group) and 6 hardwired "true" outputs are scanned out on the response bus for use by the ADC in isolating MSU faults. Bit positions 9, 22, and 23 of the program data word are ignored by the MSU.

Row and column codes, contained in bit positions 10 through 21 of the MSU program data word, are combined with the output of the MSU submatrix comparator to provide enabling of a submatrix output switch if all comparisons are true. This switch will then pass the selected analog input onto an analog measurement bus. The solid-state analog switches provide switching of both signal and return of each input signal. A quad arrangement of the switches for each input and return channel assures removal of input signals if one switch fails to open when its channel address is removed from the data holding register. Out of each 36 input channels, 12 are four-pole, dual quad, configurations to provide for two-signal time-interval and phase measurements. A second analog measurement bus is provided to accommodate these two-signal type inputs. The measurement busses route the selected analog input signals to the OCS Measurement Unit.

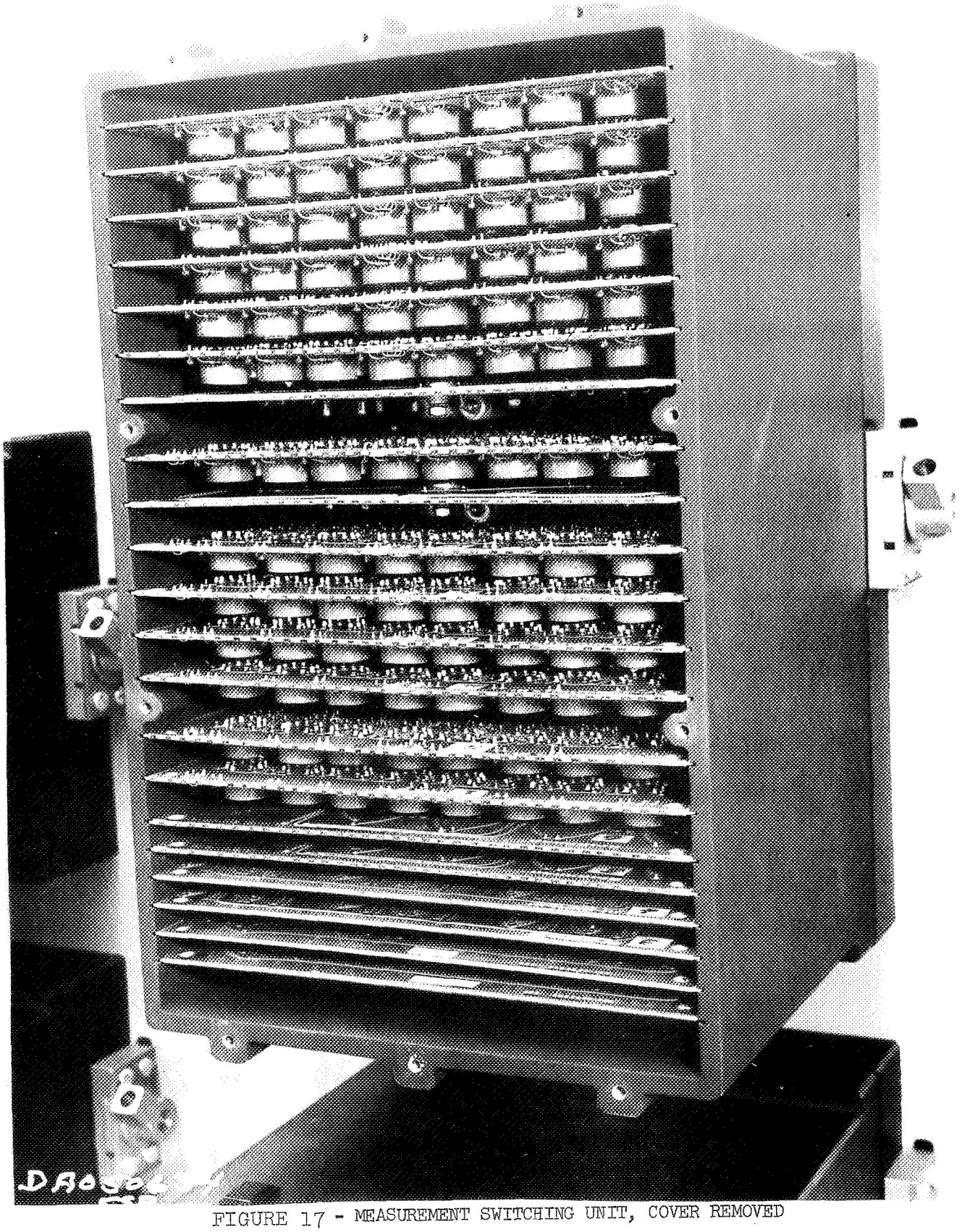


FIGURE 17 - MEASUREMENT SWITCHING UNIT, COVER REMOVED

Signal isolation between MSU input channels is 100 decibels or greater at signal frequencies to 4 KHz. Above 4 KHz the isolation decreases by not more than 17 db per decade of frequency increase.

The measurement switch unit met all of its design goals with the exception that the solid-state switch design manifested an undesirable chopper component on the signal lines. This chopper noise was typically on the order of 5 mv to 30 mv p-p, at a base frequency of 1 MHz with components extending out to approximately 20 MHz. This chopper noise did not prove to be a significant system limitation because it does become attenuated by line capacity and is rejected to a degree by the measurement unit. With low source impedance inputs this noise is essentially reduced to zero. The two most significant elements in controlling this noise are transformer balance and circuit capacity. To assist in transformer balance a phasing provision has been incorporated in the circuit layout. The noise can be reduced to half by eliminating the metal core circuit cards in favor of glass cards.

The dual emitter switch design was selected over FETS and optical devices for a number of reasons. At the time of this design, those FET switches which had sufficient breakdown voltage had intolerably high "on" resistance, while the optical deivces were unproven for reliability and too slow for this amplification.

The dual emitter switch used was a Crystallonics 3133. A uniquely designed 6 winding transformer was required for each switch since two 3N133's were used in each leg and both incoming lines were required to be switched. The other two windings were employed on the primary side: one for "close" and one for "open".

No failures have occurred to date on the MSU.

As in the case of the SSU, if MSU I/O wiring could be changed from shielded wire, the weight and fabrication complexity could be reduced.

J. SOFTWARE

There are two software systems executed by the ADC; a Spaceborne Executive Control System (SECS) and a Test Oriented Onboard Language (TOOL). These provide completely for all "on-line" operation of the OCS. In addition, two other systems are provided for off-line operations and are executed by supporting computers. These are: a Peripheral Interchange Processor (PIP), and a Program Preparation System (PPS). A general description of each software system and developmental results follows:

a. Spaceborne Executive Control System

SECS provides the operating environment for TOOL. Its functions include interrupt supervision, I/O supervision, central processor unit (CPU) scheduling, utility services and other processing environment supervision. SECS is also capable of supporting other systems besides TOOL, allowing for expansion of OCS to handle other functions such as data management.

SECS is comprised of four subsystems: an Interrupt Subsystem, a System Scheduling Subsystem, a Utility and Services Subsystem, and an Initialization Subsystem.

The Interrupt Subsystem responds to interrupts reported by the DIACU to save and restore the status of the computer, to process the interrupts, and to return control to the appropriate function upon completion of processing.

The System Scheduling Subsystem controls the execution of scheduled systems and provides services which aid in the execution of these systems.

The Utility and Services Subsystem provides common functions for the other OCS software. Included in these functions are: storage reserve and allocation; input/output service for CADU keyboard interpretation and display driving; data conversion services needed to convert the various forms of input data into binary data for use by the computer and to format binary data for the various outputs; and mathematical services required by the software.

The Initialization Subsystem provides all system initialization functions required by the software.

The information flow between the SECS subsystem is shown in the block diagram of Figure 18 . For detail information on the SECS, refer to the OCS Software Documentation, Overall Specification - Level 2, Spaceborne Executive Control System (MCR-69-194) and the SECS Subprogram Specifications listed in the bibliography of Appendix A.

The SECS system without utilities required 536 words of core memory. The utilities required 2707 words of core memory. The SECS system was implemented with the OS360 Model F assembler.

In order to optimize the utilization of the 360 system in terms of machine time and maximize confidence in a given SECS module once it was debugged, the SECS system was broken down in Control Sections for assembly. Each control section can be individually assembled, link edited and stored in data set format on the disk. When a total SECS system is required, the proper library control sections are called off of the disk library and post edited into an absolute load module.

Theoretically the above approach is excellent. However, in practice, the debugging of a control section is complicated by the fact that the programmer must, with paper and pencil, calculate relocation constants in order to trace program bugs. The edit map of course is supplied to map external symbols and control sections.

SECS represents a cross fertilization of the DTS executive and work done by IBM on the MOL executive control system.

SECS implementation is highly modular and general. This, of course, is a basic ingredient of an Executive Control System. However, generality was not carried to the point of diminishing returns. Interrupts were processed quickly and the scheduler was given control only when signaled a change in schedule status.

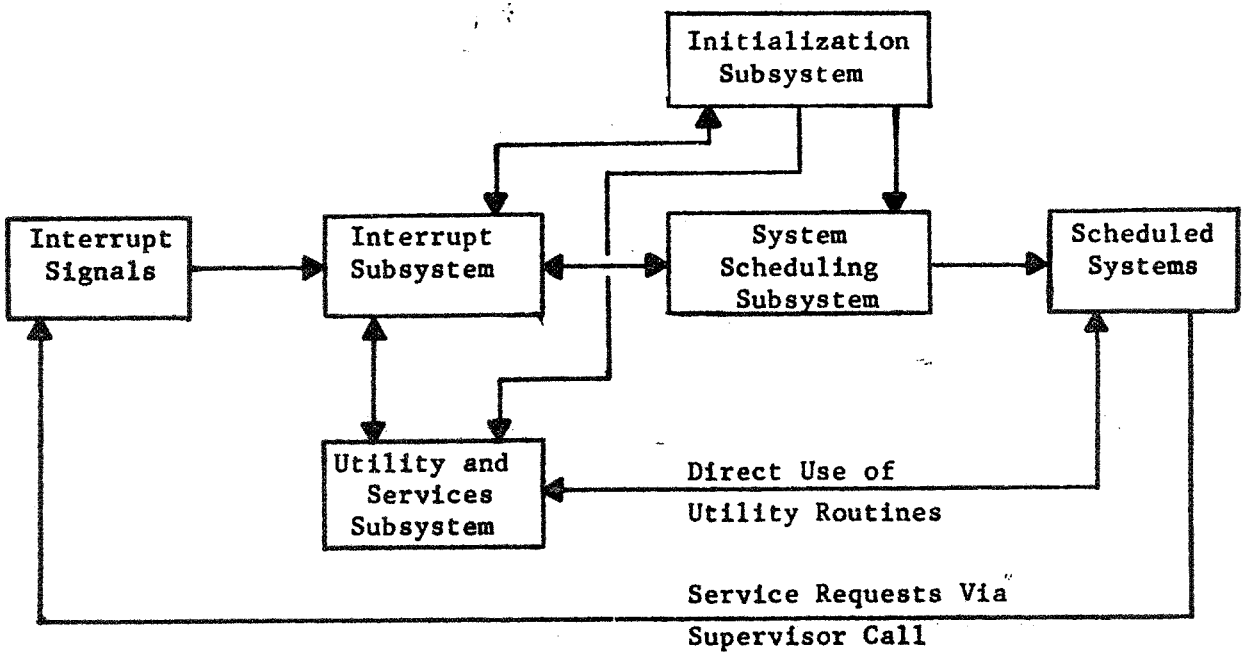


FIGURE 18 - SECS INFORMATION FLOW

The SECS system met all of its design goals such as library modularity expandability and efficiency. These were all literally tested in the course of attaching user programs and changing requirements.

In the course of evaluating SECS at NASA MSC, it was determined that memory requirements for OCS required both core and disk memory. SECS should be extended to provide dynamic memory allocation and memory overlay capability. Due to SECS modularity, this extension, even though complex, is straight forward.

Test Oriented Onboard Language (TOOL)

The purpose of this system is to provide for test execution and to allow the test engineer to write or review a test from the Control and Display Unit (CADU). TOOL is designed to operate with SECS.

Test execution is accomplished with a set of interpretative test element subroutines or "processors" which interpret a "test sequence data list". The list contains test "elements" and their "modifiers" which specify unique operations. The test sequence data list is contained in a "test procedure file".

The write/review or "test translation" capability of TOOL allows the test engineer, astronaut, or ground control to create, delete, or edit a test sequence list.

The most salient characteristic of TOOL is that test sequences are <u>data lists</u> rather than conventional computer code, thus providing an approach to higher confidence in computer code, memory savings, and easy on-line sequence modification.

Test translation consists of converting operator inputs, from the CADU keyboard, into a test sequence data list. The operator inputs are responses to "cues" displayed on the CADU. The operator may construct an entirely new test, or by utilizing the "review" capability, modify an existing test. Test execution is accomplished by the test element processors. These processors interpret the contents of the test sequence data list to perform the desired "element" operations.

Figure 19 illustrates the test structure used in the OCS checkout operations: The test element is the basic unit of the OCS test language. Each element performs a specific operation such as commanding an SSU switch closure, generating an SGU output, etc. Associated with each element is a set of modifiers. These modifiers serve to amplify the element to specify uniquely the required operation. An element may be uniquely identified by a numerical prefix, the purpose of which is to define a reference point for branching and looping within a test sequence.

A test sequence is a collection of test elements arranged in a logical order to accomplish a specific testing or control function. A test sequence can be dependent on other sequences. Hence, one sequence can set up a test and another perform the test.

"Task" is the name given to the highest level of OCS test operation. A task may be a single sequence or a series of "calls" to other sequences. There is no real difference between the structure of a task and that of a sequence.

There are four methods by which sequence execution may be initiated:

1) Manually: where the operator selects and initiates sequences through the CADU keyboard.

2) Clock: where selected sequences are initiated automatically as specified real times.

3) Monitor: where sequences are repeatedly initiated at a specified cyclic rate.

4) Remote: where the sequence is initiated from a station external to the OCS.

A sequence can be executed at any one of four independent levels which can operate concurrently.

A sequence is assigned to one of these levels during execution initiation. Associated with each level is a "priority counter" which determines the number of elements a level will execute before transferring control to another level. If a particular level is not executing a sequence it is removed from the execution cycle. Since all sequences share the same OCS resources, element execution must wait whenever a required resource is not available because it is being used by a sequence on another level of execution. Also, the time to execute a sequence will vary depending upon the number of execution levels active.

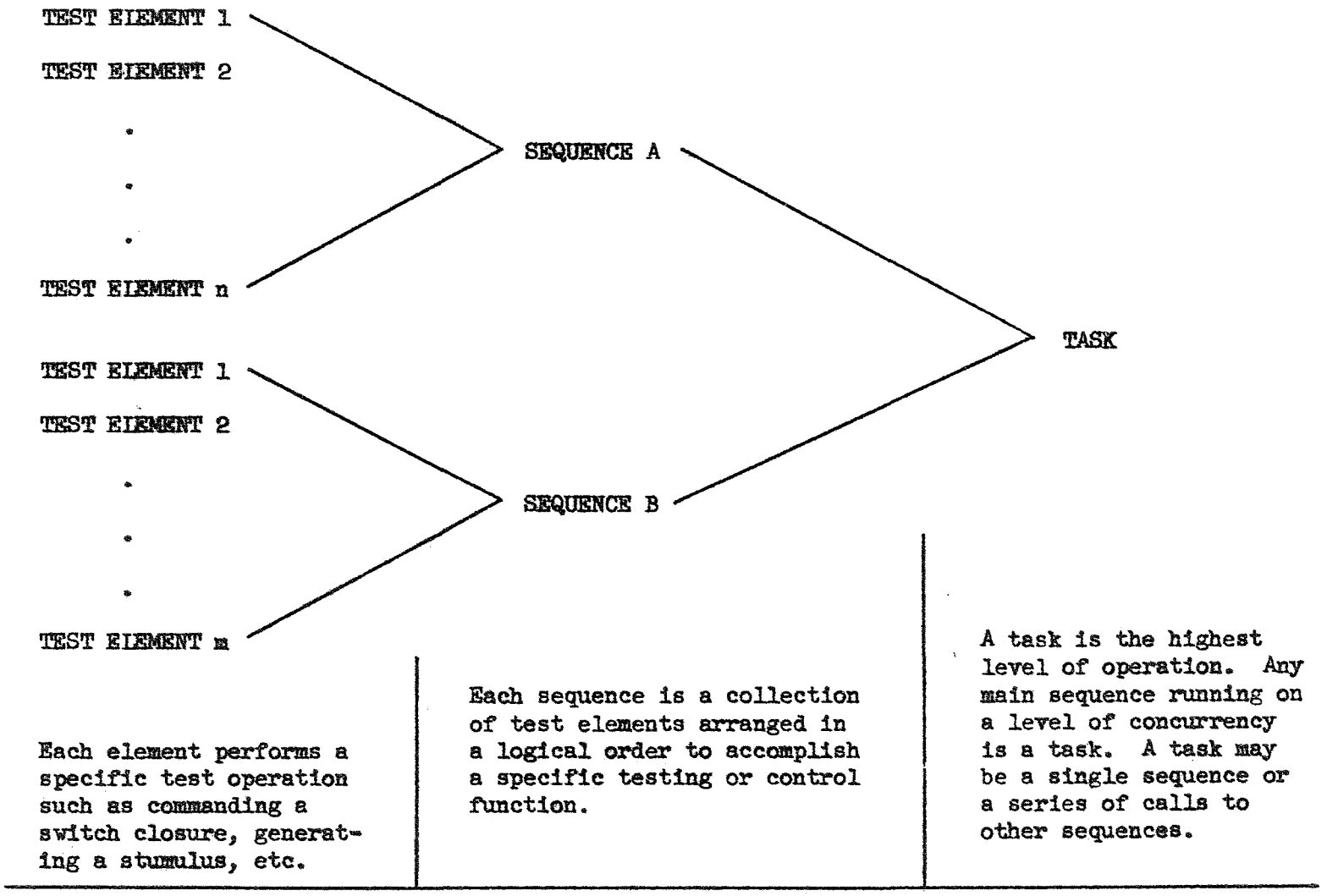


FIGURE 19 - TOOL TEST STRUCTURE

A sequence can be executed in two different modes: "continuous" or "segment". The primary difference between these modes is in the execution of the "display" element. In the segment mode all display elements encountered in a sequence are executed. In the continuous mode only specially designated display elements are executed. Since element execution stops on all display elements except "milestone" tyep, and waits for an operator response before continuing, the test writer should be careful that display elements designated for execution in the continuous mode are only those reporting an abnormal test result, reporting test program milestones, or requesting the operator to take a control action or make a keyboard input. The "segments" in the segment mode are defined by the display elements that stop execution and by the ends of sequences.

An operation called Read Monitor Status is executed in a modified form of the segment mode. The difference being that in this operation only those sequences that have a change in "monitor status" are executed.

TOOL allocates the OCS resources by assigning the available hardware and software resources to various functions only for the time that they are required. Thus, a particular resource, such as the MU, is not tied up by a single sequence but passes from level to level as needed.

There are two categories of resources in the OCS: hardware and software. The hardware resources are: SSU, SGU, MU, MSU, DIACU timers, and CADU displays. The software resources are the four levels of sequence execution. Level A is dedicated to monitor initiated sequences when they are enabled. Level B is dedicated to clock initiated sequences when they are enabled. When either of these initiations is disabled (by operator control from the CADU), the respective level becomes an allocatable resource.

Whenever an element requires a resource it tries to allocate that resource. If the resource is available, the element is executed. If the resource is not available, control is transferred to the next active sequence execution level. On the next level cycle, the element again tries to allocate the resource and the operation is repeated.

Further details on TOOL are given in the OCS Software Documentation, Overall Specification - Level 2, Test Oriented Onboard Language System (MCR-69-192). That document contains detailed descriptions of the TOOL test elements (with examples) and a discussion of TOOL provisions that prevent improper or unauthorized execution or alteration of test sequences.

The TOOL system, like SECS, was implemented with the OS360 Model F assembler, and divided into control sections. Even though efficient implementation of TOOL was important the main emphasis was to address the test engineer or astronaut usability emphasis. This presents somewhat of a dilema between powerful capability and simplicity.

After the initial TOOL system was designed without test concurrency a detailed MMC/NASA review indicated a need to implement a four level test concurrency capability. This was the final TOOL system approach.

Two significant design problems were presented by concurrency. The first problem dealt with utilization of the plasma display, the second with use of the OCS remote hardware resources.

The utilization of the plasma display was a problem because of the limitation of the 21 characters by 12 lines. A lenghty analysis effort was required to determine how to present the real time status of the four concurrent levels along with allowing a certain portion of the display to be used for checkout data presentation and attempt to retain an understandable man/machine interface. This was resolved by dedicating the first four lines to the four concurrent levels for status, the next six lines for test data, the next line for OCS status, and the last line for displaying the keyboard entry characters.

Since the development OCS employed only one set of stimulus and measurement equipment, a competition for resources is present when running concurrent tests. TOOL is in charge of resource allocation. The measurement equipment is de-allocated after each measurement. The stimulus equipment is de-allocated only after a test is completely terminated by the final END element.

This scheme offers the best guarantee to test continuity and resource sharing.

With the addition of more OCS remote units this dilema will approach resolvement. The allocation algorithms have proven satisfactory.

The TOOL execution system required 3858 words of core memory.

The TOOL translator for interactive manipulation of tests required 16,000 words of core memory. As a result of this core utilization, the entire OCS system cannot be loaded into the computer, and, as a result, consists of two separate core loads. One load contains the executive and execution systems and one load contains the executive and translation systems.

The TOOL translator is a two pass system with the second pass invisible to the user. The translator for DTS was a single pass type since it did not deal with the "Go To" function. The TOOL translator although fertilized by DTS is far more complex due to added capability to delete on an element basis, change any modifier without changing type, allow branching, and three times as many total elements. Also, use of the plasma display alphanumerics also took its toll on memory required.

The choice of elements for a language always is a good topic for discussion. The selection was made through MMC/NASA meetings. In the course of evaluating the OCS at MSC suggestions for new elements are being made. The trend of these suggestions has been toward more arithmetic power, finite control of the display resource and capability to file data for future use.

The interpretive structure of the TOOL system utilizing the Test Sequence Data List has, throughout DTS and OCS, been an excellent approach in terms of memory storage, write/review capability and high confidence in computer programs.

Supporting Software

OCS computer programs are prepared by means of a Program Preparation System (PPD). This system is composed of four subsystems, all of which are executed on an IBM System/360-65:

1) IBM System/360 Assembly Language

2) IBM System/360 Linkage Editor

3) IBM System/360 Post Editor

4) OCS Tape to Card

The PPS is of interest primarily to professional programmers preparing or modifying OCS software systems. PPS is provided in this report. Reference documents available from IBM are listed in the bibliography of Appendix A.

OCS computer memory loading, and system development testing are accomplished with a supporting computer system; a Control Data Corporation (CDC) 160A or 160G and associated peripherals. The software subsystem Peripheral Interchange Processor (PIP) is provided for this purpose.

The PIP system interfaces the ADC with the CDC 160 peripherals such as card reader, line printer, paper tape punch/reader, and magnetic tape units; through the CDC 160 computer. When commanded by the ADC, the PIP drives the peripheral devices; allowing loading and readout of the ADC memory from and to these peripherals.

J. PACKAGING

This was an area of prime concern to this contract. That is, it was the intention to develop an airborne package which could be employed in future OCS applications. In fact a study previously referenced (MCR-68-360) was performed to this end.

The developmental design which has been generated is a versatile packaging concept. The design is of such nature that various case sizes are readily generated. Also, arrangement of internal hardware is flexible. Four primary parts form the case: box-wall section, printed circuit board connector/component structure, baseplate and cover. The box-wall section is a welded magnesium alloy structure. The side-walls of this structure are grooved, as required by detail drawings for printed circuit cards and any compartment separations. The connector/component structure and cover are milled magnesium alloy details. The baseplate is milled aluminum alloy detail. All of these parts were black anodized per airborne requirements.

For the developmental lab unit, the printed circuit connector employed was a 100-pin solderable unit manufactured by ELCO Corporation. In a couple of usages all or nearly all of the 100 pins were used. The external interfacing connectors which mount in the baseplate were 50-pin solderable units made by Cannon.

The connector/component structure and baseplate served as the basic components of the internal wiring fixture. That is necessary connectors were mounted on each unit and then, using angle brackets, were connected together at a fixed angle for ease of working and for control of PCB connector to external connector wiring. The weight of the baseplate maintained the unit in a working location for the technician to make the wire terminations. It was found helpful to complete all printed circuit card connector terminations first.

As has been mentioned during the hardware unit discussions, three package sizes were employed by the OCS developmental hardware. For purposes of this report these have been identified as Types A, B and C. Following provides case dimensions for each type.

Type	Dimensions (in)
A	4 x 6.25 x 6.82
B	9.85 x 6.25 x 6.82
C	5.82 x 6.25 x 6.82

In conjunction with the above case design, a new printed circuit board, called metal-core was developed. The purpose of this metal core was to increase the heat dissipation of the PCB mounted components. Test results on developmental samples indicated a significant improvement. However, it is possible that some of the analog circuitry problems encountered were due to the increase of capacitance to structure by use of this board. (Development time did not allow an evaluation of this consideration.) However, for digital logic using flatpacks, this approach appears to offer a decided advantage.

III. OCS/STABILIZATION AND CONTROL SYSTEM INTEGRATION (SCS)

The purpose of this integration effort is to allow the OCS to control and monitor operation of the SCS in order to provide a laboratory demonstration of the capability of the OCS and to evaluate the OCS in this role.

At this point in time, concrete data on the OCS/SCS integration and evaluation is still in the preliminary stage of definition. Therefore, much of the analysis is anticipatory in nature.

The OCS hardware is connected to the SCS test points via test cable(s). In order to reach all SCS test points it is necessary that the SCS end of the test cable(s) be moved from one connector to another. OCS external interface connectors are J41 and J42 for MSU switch points and J43 and SSU switch points. SCS external interface connectors are J1 for stimulus test points and J2, J3 and J4 for measurement test points.

The integration concentrates on the attitude Gyro Stabilization test, the Rate Gyro Stabilization test and the Attitude Gyro Coupling Unit/Attitude Gyro Accelerometer Assembly test. In all tests the control circuits are exercised by the OCS and the SCS operation monitored by the OCS. Sufficient test points are monitored to verify correct operation.

Particular emphasis at this stage is placed on the writing of sequences and the effectiveness of TOOL.

During construction of the test sequences required for the above testing several refinements for TOOL were pursued.

The DISPLAY element currently clears the screen before the element is executed, hence, removing previous data. It would be useful to erase only the line which is being written. In addition, the element stops execution after a display is written. It was determined it would be helpful to allow the option of not stopping when requested.

Another discovery involved the use of the DELAY element. It seems desirable to be able to calculate a delay value in a data cell. This would be implemented by indirecting the value from a data cell.

A point of discussion and a fertile territory for future development is the hierarchy of TOOL with respect to execution. For instance, should a sequence automatically de-allocate resources when a minor END element is executed? This discussion is precipitated by use of multiple CALLS.

A concern during writing the status monitor sequences was that of the OCS status monitor philosophy. This philosophy places maximum emphasis on status compression and minimal operator intervention. The concern involves the desire to display status summaries on the display rather than a sequence oriented summary. More investigation is necessary in this area to evaluate this philosophy.

Results of the OCS/SCS integration are itemized in the next section on recommendations.

IV. RECOMMENDATIONS

The previous parts of Section II and III have presented developmental results and evaluations of the OCS components. Recommendations for areas of change and areas of study which should be considered in any follow on effort are summarized below.

OCS System Approach

What does the next OCS look like?

It has become evident that no single standard data handling technique can optimally satisfy all subsystem checkout requirements.

As a result of requirements analysis done on the Apollo, Skylab, Shuttle and Station it does appear that a feasible systems approach is a hybrid of at least three techniques.

The first technique is the technique developed on OCS utilizing data on a computer demand basis with remotely located stimulus and measurement units. Closely coupled precision stimulus and measurement data requirements are best handled by this technique.

The second technique is the Data Buffer technique utilizing remote multiplexors and a central data buffer with memory map to allow automatically flagging out of limits parameters and significantly changed parameters without computer intervention. Status monitor data and parameters with low rate of change are best handled by this technique.

The third technique is the micro processor technique which provides a special purpose capability to handle high speed data, special purpose processing algorithms, and in general those requirements which cannot be handled by the other two techniques. This is sometimes referred to as built-in-test. Micro processors are often referred to as special-purpose computers.

A total checkout system would utilize all three techniques. One objective of a subsystem checkout requirements analysis would be to catagorize the data into the three techniques.

An answer to the opening question is the OCS would be a hybrid system containing the current stimulus and measurement approach, a data buffer system and appropriate micro processors. Individually these technologies have been pursued on development contracts such as the OCS but study and development work are necessary in order to establish integration techniques and tradeoffs. Two areas of focused interest are the data bus and the computer system.

There are many approaches to investigate for the data bus. Popular concepts are multiplexer format with fixed time slots, party line with each controller requesting access, a set of buses with varying capability rather than one standard. etc.

The need for a multiprocessor computer system has already been established. Techniques must be developed to optimally allocate system resources. Some of the many techniques which must be studied are dynamic memory allocation, data filing structures, CPU allocation, fail operational, and etc.

The following paragraphs relate to the OCS units developed.

Airborne Digital Computer (ADC)

- Improved program relocation hardware
- Expanded priority interrupt capability
- A subset of instructions for real-time (stack manipulation, memory to memory ops)
- Modular architecture for multiprocessor approach including memories and I/O channels
- Features for channel device-controller debug

Control and Display Unit (CADU)

- Typewriter compatible feel alphanumeric keyboard
- Plasma display with selective erase of characters
- Improvements in the Free Electron Source for plasma ignition
- Microdata assembly with more development on lens, film gate and light source.

Data Interchange and Control Unit (DIACU)

- The comment applies to all units but in specific the DIACU. Implement with LSI logic or hybrid thick film circuits

Power Conditioning and Data Control Module (PC/DCM)

- MSI of data control module. This package would include isolation transformer
- Better isolation technique for power conditioning such as isolation of switching circuitry more ideal ground path, and reduction in signal paths to reduce inductive effects

Stimulus Generator Unit (SGU)

- A packaging approach with minimal parasitic capacitance in sensitive areas.
- The output leads from the final drive stage of the output amplifier were long and passed through a connector to permit heat sink mounting of the final stage transistors. The feedback loop should be closed through the same connector. This would improve the rise time considerably.

Measurement Unit (MU)

- A requirements analysis to determine if the MU bandwidth can be reduced. This would allow significant size reduction in the signal conditioning circuitry.
- Further development of the peak detector to reduce noise susceptibility.

Stimulus Switch Unit (SSU)

- Investigation of ways to reduce size, such as elimination of shielded wire in the backplane wiring
- Convert the logic to MSI or LSI

Measurement Switch Unit (MSU)

- Review the switching requirements and conduct a new industry search to determine the optimum design approach for the switch.
- Convert the logic to MSI or LSI.
- Attempt to eliminate the shielded switch I/O wiring within the unit.

Software

- In order to reduce core memory requirements investigate a disk overlay scheme.
- Modify the DISPLAY element to allow display without erasing previous displays and without halting test sequence execution.
- Modify the DELAY element to permit indirection of the dealy value from a data cell.
- Add the following elements

  1. Print - hardcopy of test results
  2. Record - data on magnetic tape
  3. File - data on disk storage

- Investigate elements to permit processing of data arrays for tasks such as trend analysis and statistical manipulation.
- Investigate an element to provide graphic display capability.
- Investigate implementing TOOL with a common high level language such as PL-1.
- Investigate the TOOL hierarchy of element, sequence, and task, etc., to determine their execution constraints.

APPENDIX A

DOCUMENTS PERTINENT TO OCS DESCRIPTION

1. MMC DRAWINGS

a. Top Level Reference Drawings

836-0000000	Onboard Checkout System
836-0000007	OCS Wire List
836-0000008	OCS Interconnection Reference Designations
836-0000451	Power Distribution

b. Top Level Mechanical Assemblies and Details

836-0000100	Top Assembly - Control and Display Unit
836-0000160	Stimulus Generator Unit - Details
836-0000200	Data Interchange and Control Unit
836-0000250	Measurement Unit Assembly
836-0000300	Measurement Switch Unit
836-0000350	Stimulus Switch Unit Assembly
836-0000400	Control and Power Supply Unit Assembly (PC/DCM)
836-0000440	Control Panel Assembly
836-0000550	Chiller Unit Assembly - OCS
836-0007000	Ground Support Equipment, Chassis Assembly

c. Printed Wire Board Assemblies and Schematics

Drawing numbers of the printed wire board assemblies used in each of the OCS units are listed under the physical descriptions of those units in Part II of the OCS Operation and Maintenance Manual. Refer to the appropriate subsection of Section II.A, System Physical Characteristics. These drawings each consist of the following pages and sheets:

Sheet 1 - Circuit Side of Board
Sheet 2 - Component Side of Board
Sheet 3 - Circuit Schematic
Page 1 - Parts List

2. MMC SOFTWARE SPECIFICATIONS

MCR-68-361	Overall Specification - Level 1
MCR-69-191	Overall Specification - Level 2, Mission Program
MCR-69-192	Overall Specification - Level 2, TOOL - Test Oriented Onboard Language System
MCR-69-194	Overall Specification - Level 2, Spaceborne Executive Control System
MCR-69-235	Spaceborne Executive Control System Subprogram Specifications, Interrupt Subsystem
MCR-69-236	Spaceborne Executive Control System Subprogram Specification, System Scheduling Subsystem
MCR-69-320	Spaceborne Executive Control System Subprogram Specification, Utilities and Services Subsystem
MCR-69-368	Test Oriented Onboard Language Subprogram Specifications, Tool Executive Supervisor
MCR-69-529	Test Oriented Onboard Language Processor Specifications, On-Line Translator Subsystem

3. IBM SYSTEM 360 MANUALS

A22-6810	System Summary
A22-6821	Principles of Operation
A22-6822	Bibliography
A22-6843	I/O Interface
C26-3756	Assembler Programmer's Guide
C28-6514	Assembler Language

4. IBM 4 PI-EP COMPUTER AND SYSTEM CONTROL PANEL DOCUMENTS

68-K41-006A	Partial Specification for Airborne Digital Computer
68-L12-I40	Description of Martin Maintenance Diagnostic Program
68-K41-010	System Control Panel Engineering Manual

5. MISCELLANEOUS MMC DOCUMENTS

MCR-69-475	OCS Acceptance Test Plan/Test and Inspection Procedure
CR-69-318	Microfilm Storage and Display Unit Maintenance and Operation Manual

6. CONTROL DATA CORPORATION DOCUMENTS

PD82143500	Plasma Display Subsystem Special Purpose Manual

7. MMC SOFTWARE DOCUMENTATION

MCR-68-361 Rev 1	Software Documentation, Overall Specification Airborne
MCR-69-320	Software Dcoumentation, Spaceborne Executive Control System Subprogram Specifications, Utilizes and Service Subsystem
MCR-69-529	Software Documentation TOOL, Processor Specification, On-Line Translator Subsystem

8. MISCELLANEOUS DOCUMENTS

MCR-68-295 Issues 1 thru 22	Monthly Progress Report
MCR-68-305 Issues 1 and 2	Nonmetallic Materials List and Waivers
MCR-68-360 Rev 1	Packaging Concept Report
MCR-68-389	Failure Criteria
MCR-68-406	Design Review Report - Preliminary Design
MCR-68-414	Parts Selection Report
MCR-69-192	Software Documentation, Overall Specification - Level 2, TOOL, Test Oriented Onboard Language System
MCR-69-289	Interim Reliability Prediction
MCR-69-290	Design Criteria
MCR-69-317	Design Review Report - Critical Design Review
MCR-69-387	Final Reliability Prediction Report
MCR-69-399 Rev 1	Operation and Maintenance Manual
MCR-69-475 Rev 2	Test Plan/Test and Inspection Procedure
MCR-70-54	Wire Lists
MCR-70-74	Factory Acceptance Test Report
MCR-70-82	OCS and SCS Integration Test Plan